

**School of Electrical Engineering and Computer Science
Washington State University**

EE 466: VLSI Design
 Course Website: <http://www.eecs.wsu.edu/~ee466>
 Semester: Fall 2009
 Instructor: Amlan Ganguly
 Office: Sloan 354
 Office Hours: Monday and Friday 2:00 - 3:00PM at Sloan 338 or By Appointment
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credits 3

Lecture: Monday, Wednesday and Friday 12:10 – 13:00 in Sloan 38
Textbook: N. Weste and D. Harris, CMOS VLSI Design: A Circuits and Systems Perspective. Third Edition. Edison Wesley, 2005
Prerequisites: EE 214, EE 311, EE 314, EE 324 or knowledge of digital or microprocessor design.
Catalog Course Description:

Introduction to Digital Design of integrated circuits with emphasis on high-performance (low power and high-speed)

Objectives: Students must be able to design, simulate and analyze CMOS circuits, Macros/Cells and sub-systems (data path circuits) with emphasis on high density, low power, and high-speed. Students will understand the role of computer aided design (CAD) tools in VLSI and will experiment with the most current technology/process.

Course Topics	Course Objective Students must be able to:
<i>Week 1:</i> Introduction to CMOS circuits <ul style="list-style-type: none"> - MOS transistor - CMOS Logic - Circuit representation - nMOS and pMOS transistors - MOS transistor design - The CMOS inverter (Ref: Chapter 1) 	<ul style="list-style-type: none"> • Construct gates by combining nMOS and pMOS devices. • Design circuits representing compound gates from given functions. • Design memory elements from simple CMOS devices. • Understand MOS device operation.
<i>Week 2 & 3:</i> MOS Transistor Theory (Ref: Chapter 2) <ul style="list-style-type: none"> - Enhancement pMOS and nMOS devices - MOS device design equations - DC characteristics of a CMOS inverter 	<ul style="list-style-type: none"> • Understand the importance of device parameters such as threshold voltages and their effects on device operation. • Understand the device's regions of operation and the defining equations. • Understand the effects of Noise Margin on device operation.
<i>Week 4:</i> CMOS processing Technology (Ref: Chapter 3) <ul style="list-style-type: none"> - Circuit elements - Layout Design rules - Latchup 	<ul style="list-style-type: none"> • Understand concepts related to the different CMOS processes such as n-well, p-well and twin-tub processes. • Understand the design rules. • Understand latchup issues and solutions to the problems caused by latchup.
<i>Week 6 & 5:</i> Circuit characterization and performance evaluation (Reference Chapter 4) <ul style="list-style-type: none"> - Delay estimation - Logical Effort - Power dissipation - Interconnects - Transistor sizing 	<ul style="list-style-type: none"> • Estimate resistance of non-regular regions and contacts. • Characterize MOS routing capacitances. • Understand effects of distributed RC on performance. • Understand the benefits of transistor sizing. • Understand concepts of charge sharing. • Determine/Estimate/compute power dissipated by CMOS circuits.
<i>Week 7:</i> CMOS Circuit Logic and Design (Ref: Chapt 6) <ul style="list-style-type: none"> - Physical design of logic gates - CMOS logic structures - I/O Structures - Clock 	<ul style="list-style-type: none"> • Design a gate different ways taking note of area and performance gains with each design approach. • Understand different clocking schemes such as single phase and two phase clocking schemes.
<i>Week 8 & 9:</i> Design methods <ul style="list-style-type: none"> - Design strategies - Design options (gate arrays) - Advanced design tools (capture and verification) 	<ul style="list-style-type: none"> • Understand the concepts of structured design (hierarchy, regularity, modularity and locality). • Understand gate array, full-custom etc design styles • Have knowledge of available CAD tools and verification methods.
<i>Week 10 & 11:</i> Subsystem Design <ul style="list-style-type: none"> - Adders, comparators, and multipliers 	<ul style="list-style-type: none"> • Design adders, comparators, multipliers and memories.

<ul style="list-style-type: none"> - Memories - Programmable logic arrays (PLAs) 	<ul style="list-style-type: none"> • Design programmable logic arrays.
<i>Week 12 & 13: VLSI Processor (Ref: Chapter 10)</i> <ul style="list-style-type: none"> - Datapath and control unit - Register file - Arithmetic logic unit (ALU) 	<ul style="list-style-type: none"> • Design circuits then implement the various processor modules.
<i>Week 14 & 15: Term project completion</i>	<ul style="list-style-type: none"> • Send completed term projects to MOSIS for fabrication

*Test dates are subject to change as per class agreement

Grading Scheme:

Homework	10%	Homework will be graded on the level of effort and no assignment will be accepted after the due date.
Midterm	25%	No make up tests will be given, a missed test earns a score of 0%.
Lab assignments	20%	Students will work in teams of two on the laboratory assignments, demonstrate working designs to the TA and turn in a narrative report of each lab on the due date.
Term Project	20%	This project will be assigned mid-way through the semester and milestones provided to enable successful completion of the work.
Final	25%	No make up quizzes will be given, a missed quiz earns a score of 0%.

Reasonable accommodations are available for students who have a documented disability. Please notify the instructor during the first week of class of any accommodations needed for the course. Late notification may cause the requested accommodations to be unavailable. All accommodations must be approved through the Disability Resource Center (DRC) in Administration Annex room 205, 335-1566, e-mail <mailto:drc@mail.wsu.edu> in Pullman.