# EE 466: VLSI Design

**Course Website:** [http://www.eecs.wsu.edu/~ee466](http://www.eecs.wsu.edu/~ee466)  
**Semester:** Fall 2006  
**Instructor:** Dr. Jabulani Nyathi  
**Office:** EME 504  
**Office Hours:** Monday, Wednesday and Friday 3:00 - 4:00PM or By Appointment  
**E-mail:** jabu@eecs.wsu.edu  
**Phone:** 335-1157

**Lecture:** Monday, Wednesday and Friday 12:10 AM – 13:00 in Sloan 233  

**Prerequisites:** EE 214, EE 311, EE 314, EE 324 or knowledge of digital or microprocessor design.

**Catalog Course Description:**
Introduction to physical design (layout) of integrated circuits with emphasis on CMOS digital circuits.

**Objectives:** Design and analysis of CMOS circuits, Macros/Cells and sub-systems with emphasis on compact low power, high-speed circuits and special purpose digital systems. Students will design and simulate a medium scale digital system for fabrication.

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<tr>
<th>Course Topics</th>
<th>Course Objective Students must be able to:</th>
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| **Week 1:** Introduction to CMOS circuits  
- MOS transistor  
- CMOS Logic  
- Circuit representation  
- nMOS and pMOS transistors  
- MOS transistor design  
- The CMOS inverter (Ref: Chapter 1) | Construct gates by combining nMOS and pMOS devices.  
- Design circuits representing compound gates from given functions.  
- Design memory elements from simple CMOS devices.  
- Understand MOS device operation. |
| **Week 2 & 3:** MOS Transistor Theory (Ref: Chapter 2)  
- Enhancement pMOS and nMOS devices  
- MOS device design equations  
- DC characteristics of a CMOS inverter | Understand the importance of device parameters such as threshold voltages and their effects on device operation.  
- Understand the device’s regions of operation and the defining equations.  
- Understand the effects of Noise Margin on device operation. |
| **Week 4:** CMOS processing Technology (Ref: Chapter 3)  
- Circuit elements  
- Layout Design rules  
- Latchup  
(Exam # 1)* | Understand concepts related to the different CMOS processes such as n-well, p-well and twin-tub processes.  
- Understand the design rules.  
- Understand latchup issues and solutions to the problems caused by latchup. |
| **Week 6 & 5:** Circuit characterization and performance evaluation (Reference Chapter 4)  
- Delay estimation  
- Logical Effort  
- Power dissipation  
- Interconnects  
- Transistor sizing | Estimate resistance of non-regular regions and contacts.  
- Characterize MOS routing capacitances.  
- Understand effects of distributed RC on performance.  
- Understand the benefits of transistor sizing.  
- Understand concepts of charge sharing.  
- Determine/Estimate/compute power dissipated by CMOS circuits. |
| **Week 7:** CMOS Circuit Logic and Design (Ref: Chapt 6)  
- Physical design of logic gates  
- CMOS logic structures  
- I/O Structures  
- Clock | Design a gate different ways taking note of area and performance gains with each design approach.  
- Understand different clocking schemes such as single phase and two phase clocking schemes. |
| **Week 8 & 9:** Design methods  
- Design strategies  
- Design options (gate arrays)  
- Advanced design tools (capture and verification) | Understand the concepts of structured design (hierarchy, regularity, modularity and locality).  
- Understand gate array, full-custom etc design styles.  
- Have knowledge of available CAD tools and verification methods. |
| **Week 10 & 11:** Subsystem Design  
- Adders, comparators, and multipliers | Design adders, comparators, multipliers and memories. |
<table>
<thead>
<tr>
<th>Exam # 2*</th>
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<tbody>
<tr>
<td>Memories</td>
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<td>• Design programmable logic arrays.</td>
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<td>Programmable logic arrays (PLAs)</td>
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<td>Week 12 &amp; 13: VLSI Processor (Ref: Chapter 10)</td>
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<td>• Design circuits then implement the various processor modules.</td>
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<td>Datapath and control unit</td>
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<td>Register file</td>
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<td>Arithmetic logic unit (ALU)</td>
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<td>Week 14 &amp; 15: Term project completion</td>
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<td>• Send completed term projects to MOSIS for fabrication</td>
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*Quiz and test dates are subject to change as per class agreement

**Grading Scheme:**

- **Homework** 10%  
  Homework will be graded on the level of effort and no assignment will be accepted after the due date.
- **Tests (2)** 30%  
  No make up tests will be given, a missed test earns a score of 0%.
- **Lab assignments** 20%  
  Students will work in teams of two on the laboratory assignments, demonstrate working designs to the TA and turn in a narrative report of each lab on the due date.
- **Term Project** 20%  
  This project will be assigned mid-way through the semester and milestones provided to enable successful completion of the work.
- **Final** 20%  
  No make up quizzes will be given, a missed quiz earns a score of 0%.

Reasonable accommodations are available for students who have a documented disability. Please notify the instructor during the first week of class of any accommodations needed for the course. Late notification may cause the requested accommodations to be unavailable. All accommodations must be approved through the Disability Resource Center (DRC) in Administration Annex room 205, 335-1566, e-mail mailto:drc@mail.wsu.edu@drc@mail.wsu.edu in Pullman.