

EE466: Lab Assignment 1

Due Sept 28, 2009, Monday

10 points on each question

1. NMOS and PMOS plots using Cadence Spectre.

In this exercise, you are required to generate both NMOS and PMOS I-V device characteristics using Cadence Spectre and parameters for 65nm CMOS technology. Plot your results. Let $W=0.12\mu\text{m}$ and $L=0.06\mu\text{m}$ for the NMOS device, and $W=0.24\mu\text{m}$ and $L=0.06\mu\text{m}$ for the PMOS device. Compare the current levels for the two devices in saturation.

Now connect the PMOS and NMOS transistors to form a CMOS inverter. Plot the voltage transfer characteristics, and observe the variation by varying the pull-up to pull-down device ratios by performing a parametric analysis with respect to varying width of the PMOS device. Please report the width of the PMOS for which we achieve symmetric switching. Note that this is your minimum sized transistor for 65nm technology.

2. Problem 2 uses the MOS circuit of Figure 0.7.

a. Plot V_{out} vs. V_{in} with V_{in} varying from 0 to 2.5 volts (use steps of 0.5V). $V_{DD} = 2.5$ V.

b. Repeat a using Cadence.

c. Repeat a and b using a MOS transistor with $(W/L) = 4/1$ (using the default channel length for 65nm, and $V_{DD} = 1$ V). While doing so, vary the resistance values and report the results for 16K, 32K, and 64K Ohms. Is the discrepancy between manual and computer analysis larger or smaller (perform hand calculations for only resistance of 64K)? Explain why. Also, plot the voltage transfer characteristics and comment on the noise margins. Can this circuit be used as an inverter (**bonus 2 points**)?

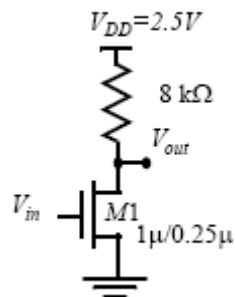


Figure 0.7 MOS circuit.