

EE466: Lab Assignment 2
Due Oct 22, 2009, Friday

10 points on each question

1. From Lab 1 you already know the ratio in 65nm technology that gives symmetric switching for a unit inverter. From theory find out what ratio should give you fastest average propagation delay. Explain with simulations in CADENCE. Find out the fan-out-of-4 delay for this gate. Is the FO4 delay lower than no load delay of this gate? Also, find out experimentally at what size of the PMOS the inverter will have lowest FO4 average propagation delay.
2. Construct a 4 input AND gate using 2 input AND gates in both tree and chain architectures. Compare the total power dissipation of these 2 circuits for all possible input transitions.