

Solutions to Practice Exam: Midterm, EE466

1 (a). (a) 0; (b) 0.6; (c) 0.8; (d) 0.8 Notice that when the gate source voltage is less than the V_t , the source-drain is swapped to make the output side the source with a V_t drop.

(b) Circuit is a buffer with degraded outputs.

Output swing calculation:

When $V_{IN} = V_{DD}$, output voltage is $V_{OH} = V_{DD} - V_{TN}$. Since the source of NMOS transistor is not connected to substrate (ground), we must take into account body effect.

When $V_{IN} = 0V$, output voltage is $V_{OL} = |V_{TP}|$. Since the source of PMOS transistor is not connected to substrate (V_{DD}), we must take into account body effect.

Therefore the output swing is $V_{DD} - V_{TN}$ to $|V_{TP}|$ with full accounting for body effect.

2(a) $C_{in} = 12$ units. $g = 1$. $p = p_{inv}$. Changing the size affects the capacitance but not logical effort or parasitic delay.

(b) The delay can be improved because each stage should have equal effort and that effort should be about 4. This design has imbalanced delays and excessive efforts. The path effort is $F = 12 * 6 * 9 = 648$. The best number of stages is 4 or 5. One way to speed the circuit up is to add a buffer (two inverters) at the end. The gates should be resized to bear efforts of $f = 648/5 = 3.65$ each. Now the effort delay is only $DF = 5f = 18.25$, as compared to $12 + 6 + 9 = 27$. The parasitic delay increases by $2p_{inv}$, but this is still a substantial speedup.

3 (a) Dynamic power consumption will go down because it is quadratically dependent on V_{DD} . Static power will go up because subthreshold leakage is exponentially dependent on V_t .

(b) The tree structure with symmetry dissipates less glitching power as all the intermediate nodes experience same delay. Whereas in the chain structure due to gate delays the inputs do not suffer the same delays causing spurious transitions due to timing mismatches.

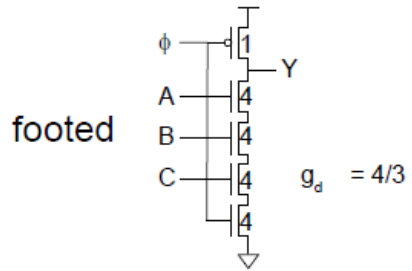
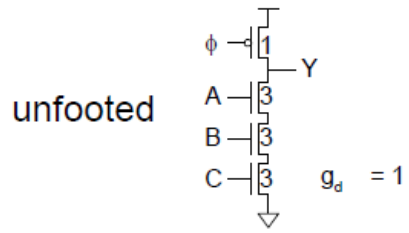
The activity factors for the tree circuit are $3/16$, $3/16$ and $15/256$ for the output.

The activity factor for the chain circuit are $3/16$, $7/64$ and $15/256$. Hence for all same gate sizes the chain circuit will dissipate more dynamic power.

4(a) $n_{crit} = 1$. For $g_{crit} = 1.5$, $C_{in} = 4.5$, so $p_{crit} = 4.5 - 1 = 3.5$ on the critical input. For unit resistance, $R = 2/p_{crit} + 2*(2/p_{noncrit}) = 1 \rightarrow p_{noncrit} = 4/(1-2/p_{crit}) = 28/3$. If $n_{noncrit} = 1/2$, $g_{noncrit} = (p_{noncrit} + n_{noncrit}) / 3 = 3.28$. n_{crit} is chosen as 1 to make the drive strength same as the unit inverter on the downward swing through the critical input.

(b)

NAND3



NOR3

