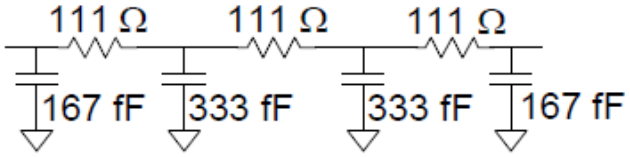
Homework 3

4.30) The wire width is 1.2 □m so the wire is 5000 □m/1.2 □m = 4167 squares in length. The total resistance is (0.08 □/sq)•(4167 sq) = 333 □. The total capacitance is (0.2 fF/□m)•(5000 □m) = 1 pF.



4.32) $R = 0.05*l/W$; $C = l*C(W, S)$; $W + S = 1000$ nm. $C(W, S)$ is found from Table 4.8. The *C*adj term is doubled if the adjacent bits might switch in the opposite direciton. If neighbors are not switching, choose $S = 320$ nm and $W = 680$ nm. If neighbors are switching, choose $S = 500$ nm and $W = 500$ nm. In the first case, resistance dominates so the wide wire is fastest. In the second case, the coupling capacitance is exacerbated by the switching neighbors, so increasing the spacing is most useful.

4.37) The gate delay component scales as S-1 to 250 ps. The delay of a repeated wire of reduced thickness scales as S-1/2 to 354 ps. The path delay scales to 604 ps, a 66% speedup.

7.2) (a) $tpd = 500 - (50 + 65 + 50) = 335$ ps; (b) $tpd = 500 - 2(40) = 420$ ps; (c) $tpd = 500 - (50 + 25 - 80 + 50) = 455$ ps.

7.8) $t_{\text{setup-flop}} = t_{\text{setup-latch}} + t_{\text{nonoverlap}}$; $t_{\text{hold-flop}} = t_{\text{hold}} - t_{\text{nonoverlap}}$; $t_{\text{pcq-flop}} = t_{\text{pcq}}$.

7.10) (a) 700 ps; (b) 825 ps; (c) 1200 ps.