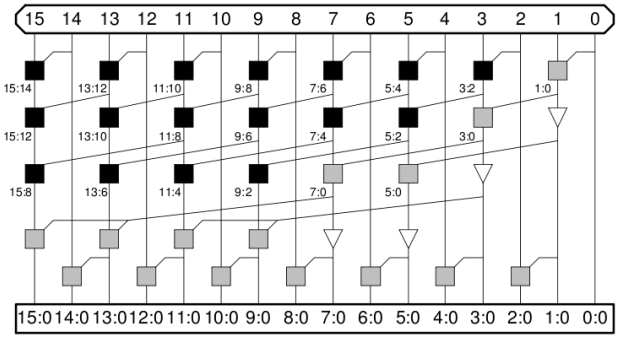
Homework 4 Solutions

10.2) Overflow for signed numbers only occurs when adding numbers with the same sign (positive or negative). The numbers overflow (V) if the sign of the result Y does not match the sign of the inputs A and B:

$$V = A_{N-1} B_{N-1} Y_{N-1} + A_{N-1} B_{N-1} Y_{N-1}$$

10.8)

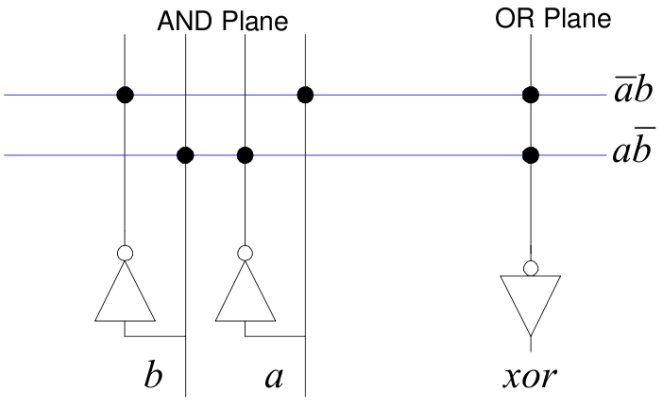
10.8



11.5) (a) B = 512. H = 20. A 10-input NAND gate has a logical effort of 12/3, so estimate that the path logical effort is about 4. Hence F = GBH = 40960. The best number of stages is log 4F = 7.66, so try an 8-stage design: NAND3-INV-NAND2-INV-NAND2-INV-INV-INV. This design has an actual logical effort of G = (5/3) * (4/3) * (4/3) = 2.96, so the actual path effort is 30340. The path parasitic delay is P = 3 + 1 + 2 + 1 + 2 + 1 + 1 + 1 = 12. D = NF1/N + P = 41.1 τ.

(b) The best number of stages for a domino path is typically comparable to the best number for a static path because both the best stage effort and the path effort decrease for domino. Using the same design, the footless domino path has a path logical effort of G = 1 * (5/6) * (2/3) * (5/6) * (2/3) * (5/6) * (1/3) * (5/6) = 0.071 and a path effort of F = 732. The path parasitic delay is P = 4/3 + 5/6 + 3/3 + 5/6 + 3/3 + 5/6 + 1/3 + 5/6 = 7. D = NF1/N + P = 25.2 τ.

11.10



11.12) NAND ROMs use series rather than parallel transistors and one-cold rather than one-hot wordlines. They tend to be smaller than NOR ROMs because they do not require contacts between the series transistors, but they are also slower because of the series transistors.