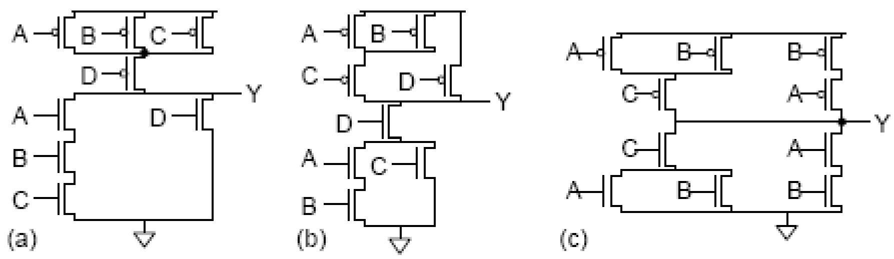
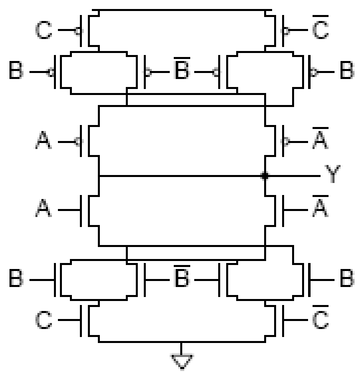
Homework 2 Solutions, EE466.

1.4)

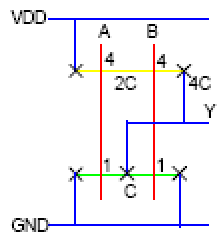


1.6)



4.2)

The rising delay is (R/2)*2C + R*(5C+5hC) = (6+5h)RC and the falling delay is R*(5C+5hC) = (5+5h)RC.



4.6)

C_{in} = 12 units. $g = 1$. $p = p_{inv}$. Changing the size affects the capacitance but not logical effort or parasitic delay.

4.10)

(a) should be faster than (b) because the NAND has the same parasitic delay but lower logical effort than the NOR. In each design, $H = 6$, $B = 1$, $P = 1 + 2 = 3$. For (a), $G = (4/3) * 1 = (4/3)$. $F = GBH = 8$. $f = 8^{1/2} = 2.8$. $D = 2f + P = 8.6\ \tau$. $x = 6C * 1 / f = 2.14C$. For (b), $G = 1 *(5/3)$. $F = GBH = 10$. $f = 10^{1/2} = 3.2$. $D = 2f + P = 9.3\ \tau$. $x = 6C * (5/3) / f = 3.16C$.

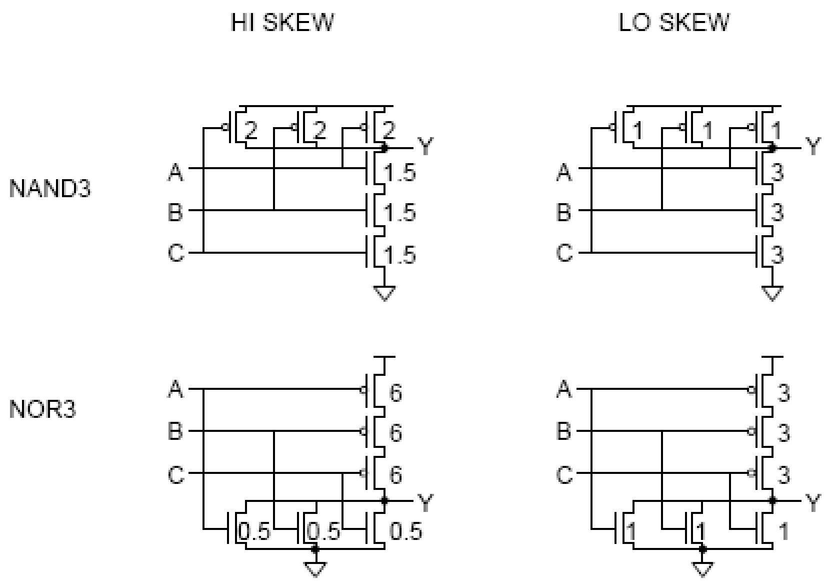
6.6)

$g = 6/3$ at the OR terminals and 4/3 at the AND terminal. $p = 8/3$.

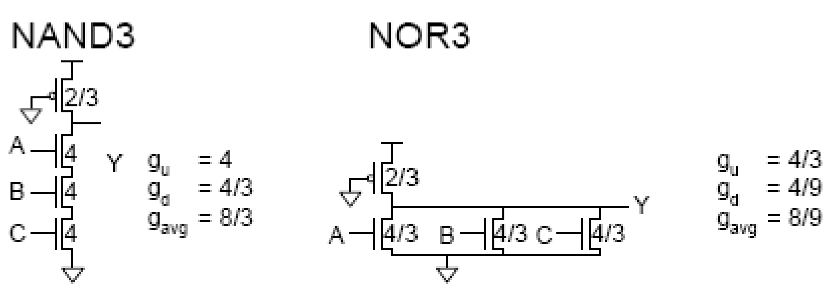
6.10)

NAND3: HI-skew: $g_u = 7/6$; LO-skew: $g_d = 4/3$

NOR3: HI-skew: $g_u = 13/6$; LO-skew: $g_d = 4/3$



6.18)



6.24)

The average logical effort is 5/4, slightly less than 4/3 for a static CMOS NOR2. The improvement is marginal and comes at the cost of contention.

6.38)

The static designs with and without complex AAOI gates use 28 and 40 transistors, respectively. The nonrestoring transmission gate design uses 16 transistors, though adding inverters on the inputs would raise that to 24 and make the mux restoring but inverting. Adding an output inverter to make the mux noninverting brings the transistor count to 26.