

EE466: Midterm
October 14, 2009, 12.10-1.00pm

Syllabus

1. MOSFET characteristics and operations
 - a. Structure
 - b. Current equations
 - c. Capacitances
 - d. Non-ideal effects
2. CMOS Fabrication
 - a. Steps
 - b. Materials
3. CMOS Inverter
 - a. Operation, zones of transistor operations
 - b. DC response (Voltage Transfer Characteristics)
 - c. Noise margins
 - d. Transient response
 - e. Delay estimation
 - i. Delay models: Elmore delay
4. Logical Effort
 - a. Optimize for minimum delay
 - b. Sizing of intermediate stages
 - c. Basically everything to do with LE!
5. CMOS Circuits and Layout
 - a. Gate design
 - i. Pullup/Pulldown network design
 - b. Pass transistors, tristates, mux, transmission gates
 - c. Latches and flip-flops
 - d. Layouts
 - i. Area estimations
6. Combinational Circuits
 - a. Bubble pushing
 - b. Input ordering
 - c. Asymmetric gate designs
 - d. Skewed gate designs
 - e. Best P/N ratio for speed
7. Circuit families
 - a. Pass transistors
 - b. Transmission gates
 - c. Pseudo-NMOS
 - d. Dynamic logic
 - e. Domino logic
 - f. CPL
8. Power Dissipation
 - a. Dynamic
 - b. Static

- c. Leakage
- d. Techniques of reducing power dissipation