

## EE466: Term Project, 2009

**Due on the day of final exam**

### **Low Swing Signaling:**

1. Study and implement in CADENCE the following Low swing interface circuits from reference paper 1 [Rabaey] on the website.
  - a. Conventional Level Converter
  - b. Symmetric Source Follower-Driver with Level Converter
  - c. Level Converting Register
2. Get the appropriate interconnect parameters, e.g., capacitance and resistance from the reference paper 2 [Saraswat] on the website.
3. Implement aggressor wires on either side of the low swing interconnect.
  - a. This can be done by loading the low-swing interconnect with appropriate Miller capacitances for the aggressors from paper 2.
4. Observe the delay from input to output for each interface circuit for all crosstalk patterns for the following lengths of the interconnects.
  - a. 5mm
  - b. 10mm
  - c. 15mm
5. Find the power dissipation of each of these cases.
  - a. Compute power-delay product and energy delay product of each of these circuits
6. Present a report on the following points
  - a. Brief description on the operation of each of these interfaces
  - b. Extraction of the interconnect parameters and construct your circuit
  - c. Study all crosstalk patterns and observe worst case and average delay on the interconnects
  - d. Find out power dissipation on all the interconnects
  - e. Present power-delay product and energy-delay product