Problem: Sub-Threshold current-voltage (I-V) characteristics of MOS devices. Using Cadence’s schematic capture tool and the analog simulator tool (Spectre), produce sub-threshold I-V characteristic curves of both nMOS and pMOS devices at the 0.18 µm technology node.

a) Make sure the maximum value of $V_{DD}$ is equal to $V_{t0}$ (obtain $V_{t0}$ from the spice parameter models).

b) From your simulations record the maximum and minimum values of $I_D$ and their corresponding gate to source ($V_{GS}$) and drain to source ($V_{DS}$) voltages.

c) Vary temperature values from 25 °C to 125 °C and monitor the changes of $I_D$ making sure to report these changes i.e. how do temperature variations affect $I_D$?

d) Based on your results above, do the devices still obey the simplistic switch assumption that digital designers rely on?

e) Comment on the positive or negative impact short channel effects would have in sub-threshold operation.

Problem 2: Compute $V_t$ for each device as $V_{DD}$ ranges from $1/2V_{t0}$ to $V_{t0}$ for the NAND gate below.

a) Size the devices for symmetric switching

b) Identify the gate’s worst case delay path and measure $I_{DS}$ for a select values of $V_{DD}$.

c) Set-up the circuit or the input patterns so that you can measure the leakage current. Comment on the ratio of the leakage current to the dynamic current. Note that you have to depend on the SPICE models for the appropriate parameters.