

EE 587**Catalog Description:**

System on Chip design and test. A course in deep sub-micron integrated circuit design and test.

Credits:

3

Offered:

Spring

Structure:

Two 1hrs 15 minutes lectures per week. For the course project substantial lab work will be involved.

Topics:

- (1) *Design and Technology trends* (Weeks 1-3) – This will give an introduction to design trends in deep submicron (DSM) era, including scaling trend, clock cycle and power issues.
- (2) *Role of interconnects in contemporary SoC Design* (Weeks 4-7) – Characteristics of wire delay in DSM will be studied. How wire delay is dominating the gate delay and what are the problems introduced by this will be covered. Importance of wire inductance will be discussed. Role of wire coupling on delay and crosstalk will be addressed. The emerging concept of crosstalk minimization through coding will be introduced. The different sub topics under this module are:
 - a. Delay in long wires and performance limitations
 - b. Interconnect coupling capacitance and its effect on wire delay
 - c. Crosstalk avoidance coding schemes (CAC)
 - d. Fault Modeling in presence of crosstalk
 - e. Interconnect Inductance
- (3) *System on chip and Platform-based design* (Weeks 8-12) – Emerging SoC design trends will be discussed. Topics covered are:
 - a. IP-based design and reusability
 - b. Multiprocessor SoC Platform Design

- c. 3D Integration
- d. On-chip Optical and Wireless Communication
- e. Design for Testability (DFT)
- f. Test Access Mechanism (TAM)
- g. Concept of core-based test & IEEE P1500 standard for SoC test

(4) ***Importance of Power and Low power SoC design methodology*** (Weeks 13-16) –

Different Low-power design methodologies will be introduced. Topics covered under this module are:

- a. Physics of Power Dissipation in CMOS
- b. Design and Test of low-voltage CMOS circuits
- c. Multiple Threshold CMOS (MTCMOS), Variable Threshold CMOS and other related methodologies for leakage power reduction
- d. Coding for low power
- e. Power minimization through architecture level optimization

Assignments:

There will be several homework and reading assignments. In reading assignments students are expected to read research papers and submit summaries. The reading list will be available on the course website. Each student will have the opportunity to present one paper to the class. Each student is expected to complete a design project. There will be one midterm and one final exam.

Project:

Each student is expected to complete a design project.

Suggested Texts:

(1) Analysis and Design of Digital Integrated Circuits - In Deep Submicron Technology, Hodges, Jackson and Saleh, McGraw-Hill, Third Edition, 2004

(2) Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits by M. L. Bushnell and V. D. Agrawal, Boston: Springer, 2005, ISBN 0-7923-7991-8

Grading:

Assignments:	15%
Paper Summary:	10%
Class Presentation:	10%

Project: 30%
Midterm Exam: 10%
Final Exam: 25%

Students with Disabilities: Reasonable accommodations are available for students with a documented disability. If you have a disability and may need accommodations to fully participate in this class, please visit the Disability Resource Center (DRC). All accommodations MUST be approved through the DRC (Admin Annex Bldg, Room 205). Please stop by or call 509-335-3417 to make an appointment with a disability specialist.

Academic Integrity: The School of Electrical Engineering and Computer Science Academic Integrity Policy will apply to this course. In summary, the policy provides that EECS faculty who observe instances of academic dishonesty, i.e., cheating, will have the full range of options available to them that are outlined in the Student Handbook (including assigning a failing grade for the course). Additionally, faculties are encouraged to report all instances of academic dishonesty to either the Graduate or Undergraduate Program Coordinators, whichever is appropriate. Students who commit acts of academic dishonesty in an EE or CptS course who have not been certified may be ineligible for certification, while certified undergraduates may be decertified. Ignorance of these consequences or of the definition of academic dishonesty in a particular class does not serve as an excuse. Students who observe acts of academic dishonesty may report their observations to the course instructor or to the Associate Director of the School.

Students are urged to become familiar with the complete policy found at <http://school.eecs.wsu.edu/Undergraduate/AcademicIntegrityPolicy/>