A Gated Clock Scheme for Low Power Scan-Based BIST

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Abstract

In this paper, we present a new low power scan-based BIST technique which can reduce the switching activity during test operation. The proposed low power /energy technique is based on a gated clock scheme for the scan path and the clock tree feeding the scan path.

1. Introduction

With the proliferation of portable battery operated devices and the drive towards low power design and low-cost light packages, the power issues for test are becoming increasingly important [1]. Until now, ad hoc solutions have been practiced in industry for considering power consumption during test. These solutions consist in oversizing power supply, package and cooling to stand the increased current during testing, or reducing the test operation frequency. Unfortunately, these solutions increase either hardware costs or test time, and may lead to a loss of defect coverage. Thereby, a number of innovative solutions have been proposed recently to cope with the power and energy problems during test [2-6]. A survey of these solutions is given in [7].

The focus of this paper is on the problem of minimizing power dissipation during scan-based BIST. Scan-based BIST architectures are very popular because of their low impact on area and performance [8]. However, scan-based architectures are expensive in power consumption as each test pattern requires a large number of shift operations with a high circuit activity. In this paper, a new scan-based BIST technique is described which drastically reduces the total energy as well as the peak and average power consumption during shift operations.

There are three main sources of power dissipation during scan-based testing. One is the power dissipated when the outputs of logic gates in the circuit switch, which is referred to here as "logic power". Another is the power dissipated in the scan path during scan operation, which is referred to here as "scan power". The last one is the power dissipated in the clock tree each time the clock makes a transition, which is referred to here as "clock power". Therefore, the total power during scan shifting includes the logic power, the scan power and the clock power. The previously proposed approaches have all focused on reducing the logic power and/or the scan power, but did not do anything to reduce the clock power. Results in [9] suggest that clock power is a significant component of the total power during testing. In this paper, we propose an approach that reduces logic power, scan power and clock power at once. The proposed low power/energy scan-BIST technique is based on a gated clock scheme for the scan path and the clock tree feeding the scan path. The idea is to reduce the clock frequency on the scan cells during shift operations without increasing the test time.

Compared with existing low power BIST techniques, our solution offers a number of advantages. The fault coverage and the IC test time, are exactly the same as those achieved with a standard BIST scheme. The area overhead is negligible and there is no penalty on the circuit performance. The proposed BIST scheme does not require any circuit design modification beyond standard scan-BIST techniques and is very easy to implement (low impact on the design time). Reductions of average logic power, scan power and clock power are up to 42%, 55% and 71% respectively for experimented ISCAS benchmark circuits.

2. The gated clock scheme

2.1 Standard test-per-scan scheme

In standard test-per-scan BIST, a Test Pattern Generator (TPG) generates a bit sequence which is fed into the scan path. The content of the scan path serves as a test pattern for the CUT. A test pattern is applied to the CUT every $m + 1$ clock cycles, where m is the number of scan cells in the scan path. The response of the CUT is captured by the scan path in parallel, and is serially scanned out during the next m clock cycles to be loaded into a Test Response Compactor (TRC); the next test pattern is scanned in concurrently. As in any scan design, each scan cell in the scan path consists of a multiplexer connected to a D flip-flop. The D flip-flop is clocked by signal CLK. Signal CLK is the clock of the circuit in the system mode and has a period equal to T. The multiplexer is controlled by signal ScanENA and allows to drive either test response data from the logic circuit (Capture Mode) or shift data from the scan input (Scan Mode) to the D flip-flop.

Figure 1 shows the timing waveforms of signals CLK and ScanENA provided by the test control unit. A logic

zero on signal ScanENA in combination with signal CLK causes stimulus data to be shifted into the scan path while response data is shifted out from the scan path. A logic one on signal ScanENA in combination with signal CLK causes response data from the logic circuit to be captured into the scan path. According to this functioning, it clearly appears that most switching activity in the circuit occurs during scan shifting. Hence, average and peak power dissipation can be reduced by first reducing the switching activity during scan operation. This reduces both the logic power and the scan power. Next, the power dissipation can still be reduced by reducing the clock power in the clock tree feeding the scan path.

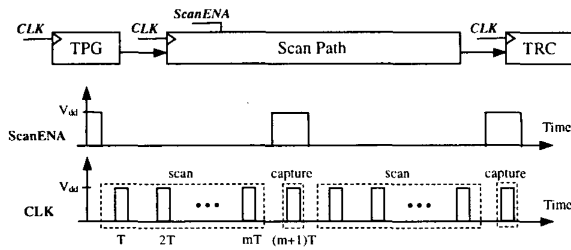

Figure 1: Timing waveforms of standard test-per-scan

2.2 Proposed test-per-scan scheme

The proposed low power scan-BIST architecture is based on a gated clock scheme for the scan path and the clock tree feeding the scan path. The idea is to reduce the clock frequency on the scan cells during shift operations without increasing the test time. For this purpose, a clock whose speed is half of the normal speed is used to activate one half of the scan cells (referred to as "Scan Path A") during one clock cycle of the scan operation. During the next clock cycle, the second half of the scan cells (referred to as "Scan Path B") is activated by another clock whose speed is also half of the normal speed. The two clocks are synchronous with the system clock and have the same but shifted in time period during scan operations (the clocks are phase shifted). During capture operations, the two clocks operate as the system clock CLK. The basic scheme of the proposed low power test-per-scan scheme with the corresponding timing waveforms are depicted in Figure 2 and Figure 3 respectively. As one can observe, a shift operation is performed at each clock cycle of the scan operation. However, either Scan Path A or Scan Path B is active during this time. During the next clock cycle, the reverse situation occurs (for example, Scan Path B is active if Scan Path A was active in the previous clock cycle). This allows the switching activity to be better distributed in time. Consequently, the average power consumed in the CUT is minimized. Moreover, the power consumed in the scan path is also minimized since only one half of the scan cells in the scan path can be activated in a given time interval. Another important feature is that the total energy consumption during BIST is reduced since the test length with the proposed test-per-scan scheme is exactly the same than the test length with a conventional test-per-scan scheme to reach the same fault coverage.

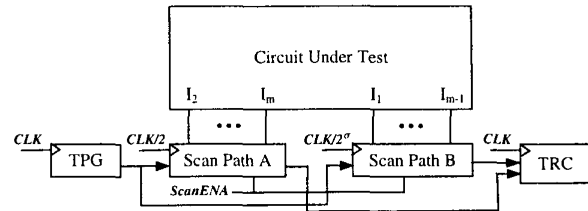

Figure 2: Proposed low power test-per-scan scheme

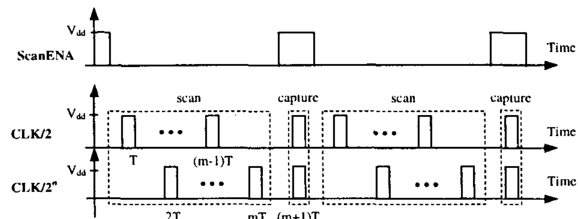

Figure 3: Timing waveforms of proposed test-per-scan

3. Complete Scan-BIST structure

The proposed scan-BIST structure is depicted in Figure 4. This structure is first composed of a test clock module which provides test clock signals CLK/2 and CLK/2$^{\sigma}$ from the system clock CLK used in the normal mode. The signal ScanENA allows to switch from the scan mode (=0) to the normal or capture mode (=1).

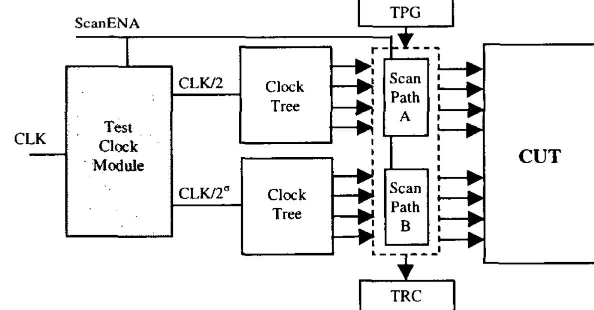

Figure 4: The complete scan-BIST structure

As two different clock speeds are needed for the scan paths, two clock trees are used in the proposed BIST scheme. These clock trees are carefully designed so as to correctly balance the clock signals feeding each part of the modified scan path. Note that using two clock trees driven by a slower clock allows to drastically reduce the clock power during BIST. Finally, the two new scan paths, Scan Path A and Scan path B, are connected to the CUT.

The test clock module which provides test clock signals CLK/2 and CLK/2$^{\sigma}$ is given in Figure 5. This module is formed by a single D-type flip-flop and four logic gates, and allows to generate non-overlapping test

clock signals (during the scan operation mode) as those represented in Figure 3. This structure is very simple (a divider followed by a demultiplexer) and requires a small overhead of hardware. Moreover, it is designed with minimum impact on performance and timing. In fact, some of the already existing driving buffers of the clock tree have to be transformed into AND gates as seen in Figure 5.

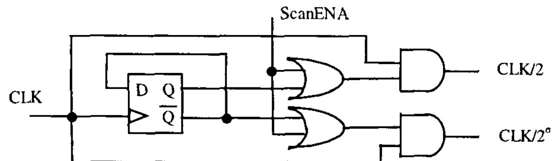

Figure 5: The test clock module

4. Experimental results

The benchmarking process was performed on circuits of the ISCAS'85 and ISCAS'89 (scan version) benchmark suites. Power consumption in each circuit was estimated by using PowerMill of Synopsys [10], assuming a clock frequency of 200 MHz and a power supply voltage of 2.5 V. Experiments performed on each circuit have been done with technology parameters extracted from a 0.25μm digital CMOS standard cell library.

Concerning experiments for the calculation of the test length and fault coverage, all experiments were based on pseudo-random pattern testing from a classical 32-bit LFSR. For each circuit, we generated 10000 pseudo-random patterns and we stopped the sequence after the last pattern which detected a new fault. *The results obtained with the proposed technique in terms of test length and fault coverage have been shown to be identical as those achieved with a standard test-per-scan BIST scheme.*

Now, results about the power and energy savings achieved by the proposed low power test-per-scan scheme are discussed. A sample of the results on logic power (power savings in the CUT) is given in Table 1. For each circuit, we have reported the peak power, the average power, and the energy obtained with the proposed low power scheme. Note that the results in energy reduction are the same as those of the average power reduction since the test length is unchanged compared with standard BIST. The complete results have shown that average power and energy reduction of up to 42% and peak power reduction of up to 36% can be achieved with the proposed technique compared to standard BIST.

Although the scan power is normally lower than the logic power, it may be not negligible, especially for circuits with a high number of inputs. In order to evaluate the efficiency of our technique in reducing this scan power, we performed another set of experiments. The results showed that our low power BIST technique reduces by roughly one half (up to 55%) the average scan power.

Circuit	peak [mW]	average [mW]	energy [μJ]	peak reduct	ave. power & energy reduct
s208	16.5	0.19	0.022	35.8%	38.2%
s510	21.8	0.56	0.031	22.3%	34.9%
s1196	73.5	2.23	3.19	9.6%	32.9%
s1488	83.3	4.47	0.94	8.6%	28.9%

Table 1: Power savings in the CUT (logic power)

Circuit	peak [mW]	average [mW]	energy [μJ]	peak reduct	ave. power & energy reduct
s208	28.6	0.33	0.038	1.2%	59.9%
s510	2.9	0.25	0.014	29.2%	70.2%
s1196	26.3	0.31	0.44	25.7%	64.7%
s1488	100.4	1.08	3.75	25.4%	49.5%

Table 2: Power savings in the clock tree (clock power)

In order to evaluate the savings in clock power, we performed a third set of experiments. Results are partially reported in Table 2. These results are based on a simple clock tree design with one buffer (or inverter) feeding 4 buffers in the next level. Note that this value is important from a design point of view but is not really important in our evaluations which have a comparison purpose. The complete results have shown that average power and energy reduction of up to 71% and peak power reduction of up to 29% can be achieved in the clock tree by using the proposed low power BIST scheme. These percentages are evaluated in comparison with a standard BIST scheme in which a single clock speed is used for the scan path.

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