Power Conscious BIST Approaches

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Abstract

The System-On-Chip (SOC) revolution has brought some new challenges to both design and test engineers. The most important challenges of today's VLSI systems testing are linked to test cost, defect coverage and power dissipation. Implementing a self-testable system may reduce test costs as expensive external high performance test equipment is not required and it may increase defect coverage as testing is performed at system speed.

Unfortunately, the classic BIST approaches lead to a significant increase of power consumption compared to the system mode and even compared to external testing. The paper will review required changes to be applied to classic BIST techniques for power reduction. A recently developed new BIST approach called functional BIST is introduced and its consequences for power dissipation are discussed.

1. Introduction

Silicon manufacturing technology improvements have facilitated the explosion in the size and complexity of modern designs. This phenomenon will continue in the next years and extreme challenges are imposed on tools and methodologies employed in the design and test of complex digital systems.

Test is currently one of the most expensive and problematic aspects in a circuit design cycle, revealing the ceaseless need for test related innovative solutions. This is confirmed by the ITRS (International Technology Roadmap for Semiconductors) statement that by 2014 it may cost more to test a transistor than to manufacture it unless techniques like logic BIST are employed [SIA99]. Logic BIST, which test logic circuits through the use of built-in pattern sources and response evaluators, offers a number of advantages compared with external testing [Wun98, Raj98, Het99, Zor99]:

- a low cost automatic test equipment (ATE) is sufficient,
- testing is performed at the maximum system speed of the device under test (DUT),
- high resolution for generating and analyzing test waveforms as no external circuitry is involved,
- lower test times by concurrently testing multiple embedded cores,
- increased defect coverage due to larger amount of test patterns applied in shorter time,
- exploiting the BIST circuitry also during system test and maintenance,
- protecting intellectual property as internal test information is not released.

BIST is nowadays a standard test method for regular structures like memories. Moreover, many CAD systems support the integration of self-test structures into random logic. In this case, test per-scan is the most widespread approach (Figure 1).

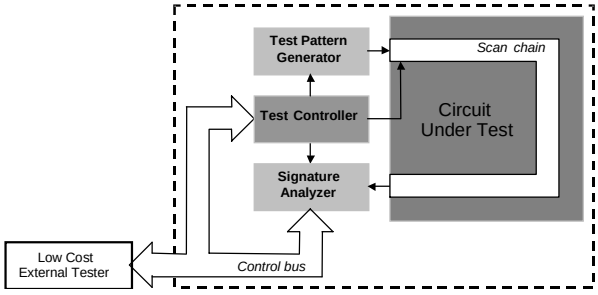

Figure 1: Test-per-scan

The core under test is equipped with one or several scan paths, the scan data inputs are connected to a hardware test pattern generator, usually a linear feedback shift register (LFSR), and the scan data outputs are fed into a signature register. Shift clocks are applied to the scan paths and the LFSR until the scan paths are filled with

test patterns. Then a system clock is applied and the test response is captured in the scan path.

The scan path content is compressed sequentially by the signature register, and a new pattern is shifted in at the same time. The test per-scan approach is compatible with standard scan design and is easily implemented, its main drawback is a rather long test application time due to its serial nature.

Test times are reduced by parallel BIST approach (Figure 2).

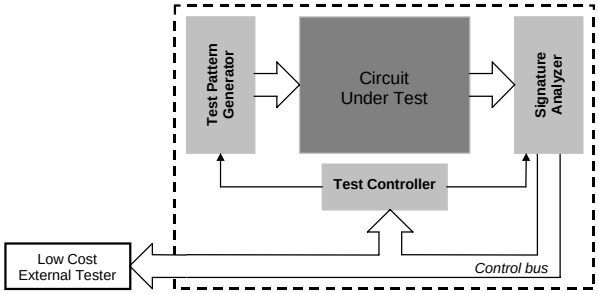

Figure 2: Test per-clock

All or some of the system registers are enhanced so that they perform in four different modes:

1. System register
2. Parallel pattern generator
3. Parallel signature register
4. Shift register

The complete test is partitioned into test sessions, in each session some registers perform pattern generation and the others work as signature register. Finally, the content of all the registers is considered as a signature and is shifted out.

Since now a new pattern is applied at each clock, testing is much faster than test per-scan testing. On the other hand, the core-under-test is modified to a larger extent with additional costs in terms of hardware overhead and performance.

Recently, the test problem caused by microprocessor complexity has been addressed [Bie95, She98, Hel96, Dor98, Che00]. The proposed solution, functional deterministic BIST uses the microprocessor functionally in order to implement a self-test for structural faults and defects. The consideration of structural faults is the main difference to classic functional test, which has already been done for a long time without a structural fault model. The advantage of this approach consists in an at-speed test for structural faults without any penalty in terms of additional hardware and performance (Figure 3).

The two first BIST approaches, test per-scan and test per-clock will result in an increased power consumption that may easily be a multiple of the power used delivering system mode [Wan97]. In contrast, the functional BIST approach will keep power consumption values in the range of the system specifications because tests are applied in the normal operation mode instead of an additional test mode.

There are several reasons for the increased test power. First, the test efficiency is correlated with the toggle rate; hence in the test mode, the switching activity of all nodes is often several times higher than the activity during normal operations. Second, in a SOC, concurrent testing is frequently employed to reduce the test application time, which may result in excessive energy and power dissipation. Third, the design-for-testability (DfT) circuitry embedded in a circuit to reduce the test complexity is often idle during normal operations but may be intensively used in test mode.

Finally, all the means of low power design as gated clocks e.g. have to be switched off as testing is just the observation of activities. The test power problem is magnified for dedicated low power designs, and the difference between power consumption during BIST and during system mode does not allow at-speed testing any more. The goal of this paper is to present means for reducing the power consumption in all the three BIST approaches: test-per-scan, test-per-clock, and functional BIST.

The remainder of this paper is organized as follows. Section 2 introduces the terminology and the power modeling used. Section 3 presents the contribution made in both scan environment and test pattern generation, Section 4 gives an introduction into the field of microprocessor testing under power constraints.

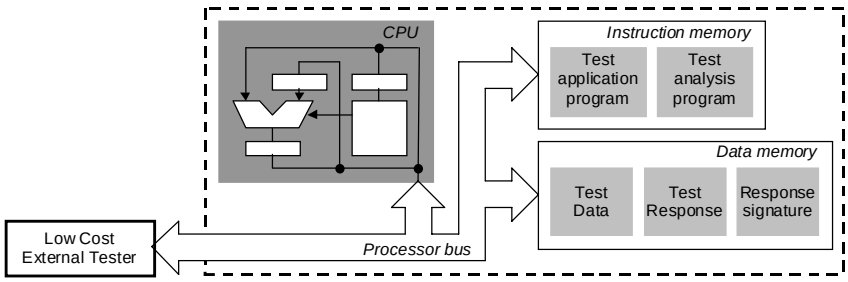

Figure 3: Functional BIST

2. Terminology and power modeling

Power consumption in CMOS circuits is classified into static and dynamic. Static power dissipation is due to leakage current or other current drawn continuously from the power supply. Dynamic dissipation is due to (i) short circuit current and (ii) charging and discharging of load capacitance during output switching.

For the recent CMOS technologies, dynamic power is the dominant source of power consumption, although this may change for future developments. The average energy consumed at node i per switching is $½ \cdot C_i \cdot V_{DD}^2$ where C_i is the equivalent output capacitance and V_{DD} the power supply voltage [Cir87]. Therefore, a good approximation of the energy consumed in a period is $½ \cdot C_i \cdot s_i \cdot V_{DD}^2$ where s_i is the number of switchings during the period.

Nodes connected to more than one gate are nodes with higher parasitic capacitance. Based on this fact, and in a first approximation, capacitance C_i is assumed to be proportional to the fanout of the node F_i [Wan96]. Therefore, the energy E_i consumed at node i during one clock period is estimated by:

$$E_i = \frac{1}{2} \cdot s_i \cdot F_i \cdot C_0 \cdot V_{DD}^2$$

if C_0 is the minimum size parasitic capacitance of the circuit. According to this expression, estimating the energy consumption at the logic level requires the calculation of the fanout F_i and the number s_i of switchings at node i. The fanout of the nodes is defined by the circuit topology, and a logic simulator may estimate the switchings. The product $s_i \cdot F_i$ is named Weighted Switching Activity (WSA) of node i and represents the only variable part in the energy consumed at node i during the test application.

According to the above formulation, the energy consumed in the circuit after applying a pair of successive input patterns (V_{k-1},V_k) may be expressed by:

$$E_{V_k} = \frac{1}{2} \cdot C_0 \cdot V_{DD}^2 \cdot \sum_i s(i,k) \cdot F_i$$

where i ranges all nodes of the circuit and $s(i,k)$ is the number of switchings provoked by V_k at node i. Assuming a pseudo-random test sequence of length L, where L is the test length required to achieve the targeted fault coverage, the total energy consumed in the circuit during application of the complete test sequence is:

$$E_{total} = \frac{1}{2} \cdot C_0 \cdot V_{DD}^2 \cdot \sum_k \sum_i s(i,k) \cdot F_i$$

Let us denote the clock period as T. By definition, the instantaneous power is the power consumed during one clock period. Therefore, the instantaneous power consumed in the circuit after application of a pair of patterns (V_{k-1},V_k) may expressed as follows:

$$E_{inst}(V_k) = \frac{E_{V_k}}{T}$$

The peak power consumption corresponds to the maximum of the instantaneous power consumed during a test session. It corresponds to the highest energy consumed during one clock period, divided by T. More formally, it may be expressed as

$$E_{peak} = \max_k P_{inst}(V_k) = \frac{\max_k (E_{V_k})}{T}$$

Finally, the average power consumed during the test session is the total energy divided by the test time L, and it given as

$$E_{ave} = \frac{E_{total}}{L \cdot T}.$$

Note that this model for power and energy consumption is rough and simplified, but it is completely sufficient for the intended purpose of power analysis during test.

3. Power consideration during BIST

3.1 State of the art

Academic research on low power design and on BIST has been performed nearly independently, while the industrial practice has required ad-hoc solutions for reducing power consumption during BIST [Mon97]. Solutions realized in practice include:

- Oversizing power supply, package and cooling to resist the increased current during testing. Breaks are inserted into the test process for avoiding hot spots.
- Test with reduced operation frequency.

The first solution increases both hardware costs and test application time. The second proposal uses less hardware, but the reduced system frequency increases test application time and may lead to a loss of defect coverage as dynamic faults may be masked. Moreover, this solution reduces the power consumption at the expense of a longer test time, but does not reduce the total energy consumption during test, which is important for the lifetime of the battery for portable equipments.

The industrial need initiated academic research. Therefore, techniques to cope with the power and energy problems during BIST have appeared

recently. These approaches can be classified as follows:

- *Distributed BIST Control Schemes* [Zor93, Cho94]. The goal in these approaches is to determine the BISTed blocks of a complex design to be activated in parallel at each stage of the test session in order to reduce the number of concurrently tested modules. The average power is reduced and consequently, the temperature related problems are avoided by the increase of the test time duration. On the other hand, the total energy remains constant and the autonomy of the system is not increased.
- *Low Power Test Pattern Generators* [Wan97, Wan99, Zha99, Cor00]. TPGs based either on LFSRs or Cellular Automata (CA) are carefully designed to reduce the circuit activity, thus reducing power consumption. These approaches effectively reduce power during the test phase but sometimes at the expense of sub-optimal fault coverage and without reduction of the peak power consumption.
- *Vector Filtering Architectures* [Gir99a, Man99, Cor99]. As each vector applied to the CUT consumes power whereas not every vector generated by the pseudo-random TPG contributes to the final fault coverage, the vector filtering architectures consist in preventing application of non-detecting vectors to the CUT. These approaches are very effective in reducing power without reducing fault coverage, but do not preserve the CUT from excessive peak power consumption and can lead to high area overhead.
- *Circuit Partitioning for Low Power BIST* [Gir99b]. This approach consists in partitioning the original circuit into structural sub-circuits so that each sub-circuit can be successively tested through different BIST sessions. When partitioning the circuit and planning the test session, the average power, the peak power and the energy consumption during BIST are minimized at some expense in terms of area overhead. One drawback of this approach is that it requires circuit design modification and causes performance degradations.

The first two techniques prolong test time and affect only a small portion of the power consumption, the last two techniques have a rather impact on hardware and performance. In the subsequent subsections more efficient solutions are proposed for the test per-scan and test per-clock BIST schemes. For the first one, the proposed solution consists in modifying a standard scan design in order to decrease the switching activity during shifting patterns. This solution is completed by a counter allowing to remove the redundant patterns of the test sequences. The second one, in a test per-clock environment, consists in modifying the clock scheme of the pseudo-random test patterns generator in order to reduce the switching activity. These different approaches are explained in the following parts.

3.2. Low power test per-scan environment

Scan design, in a full or partial version, involves high power consumption due to the shift phases. In addition, this switching activity is needless for the test quality. In order to reduce this power problem, a new technique, called toggle suppression has been proposed in [Ger99].

During shifting the output of each scan element is highly active, causing a large power consumption, whereas capturing the test response accounts only little to the total power consumption. The total power consumption dissipated in the MUT can be dramatically reduced when using a modified shift register, which suppresses the activity at output of each scan element during shift operation, as proposed in [Zel98]. The equivalent structure of a NOR stabilized shift register is shown in Figure 4.

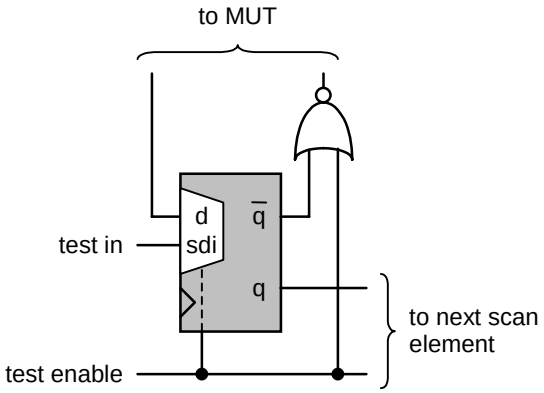

Figure 4: Scan path element with reduced output activity

The scan path element receives its input either from the MUT via *d* or from the previous scan element via *sdi*. These two modes are controlled by the test enable signal *t*, and only if the test is disabled (*t=0*), the NOR gate is transparent. If the scan path contains *n* flip-flops, *n* shift clocks and one system clock have to be applied. For these $n+1$ clocks the NOR-gate allows at most 2 signal changes, and on average we may expect only one. Without the NOR gate, *n* signal changes may occur, and on average we have to expect $(n+1)/2$ signal changes.

The NOR gate may be integrated with the latch so that just the output inverter of the latch is substituted by the NOR. In this case the performance degradation by this method is negligible.

In order to reduce the energy consumption caused by switching the clock tree and shifting irrelevant patterns into the scan path, the toggle suppression design is completed by a technique allowing to block the shifting process for all unused patterns generated by the test pattern generator. This is done by disconnecting the TPG from the scan path for all test patterns that would not detect new faults in the MUT. Thus, the fault coverage is not affected, but the energy consumption can be reduced significantly. A gating signal is derived from a decoding logic fed by the output of the pattern counter, which we assume to be present in every test-controlling unit. The resulting test design is shown in Figure 5. Only if the pattern counter indicates a useful pattern, the decoding logic enables the shift clock to the scan path. As long as this pattern is applied to the decoder, shift clocks are applied to the scan path. After filling the scan path another clock is applied in system mode and increments the pattern counter, which in turn applies a new pattern to the decoder. This new pattern index will enable or disable the shift clock for this pattern.

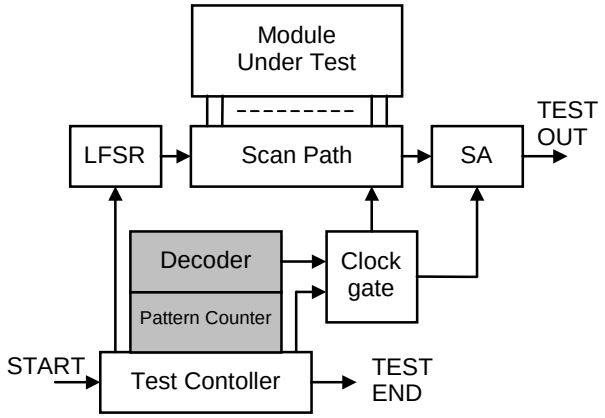

Figure 5: Scan path design with decoder for shift and system clock gating.

The results obtained in terms of power reduction if both techniques are combined are very attractive. On average, approximately 2% of the original average power are required if both methods are combined. In addition, combining both approaches especially is attractive if not all of the flip-flops are allowed to be masked by NOR gates due to timing reasons. In this case, gating the shift clock still provides reductions without penalties of performance and fault coverage. The results in terms of energy, average power and peak power reduction can be found in [Ger99].

3.3. Low power test per-clock environment

The reduction of the power consumption in a test-per-clock BIST environment is commonly achieved by reducing the switching activity in the CUT. Furthermore, in [Wan97] it has been demonstrated that the switching activity in a time interval *(i.e.* the average power) dissipated in a CUT during BIST is proportional to the transition density at the circuit inputs. Thereby, several low power test pattern generators have been proposed to reduce the activity at circuit inputs. Among these techniques, the DS-LFSR proposed in [Wan97] consists in using two LFSRs, a slow LFSR and a normal speed LFSR, as TPG. Inputs driven by the slow LFSR are those which may cause more transitions in the circuit. Although this technique reduces the average power consumption while maintaining a good fault coverage level, the peak power consumption cannot be reduced in practice (a full bit changing may occur at circuit inputs every *d* clock cycles where *d = normal clock speed / slow clock spee*d). This point represents a severe limitation of the method as the peak power consumption is a critical parameter that determines the electrical limits of the circuit and the packaging requirements.

As in [Wan97], the low power/energy BIST technique proposed in [Gir01] is based on a modified clock scheme for the pseudo-random TPG. Basically, a clock which speed is half of the normal speed is used to activate one half of the D flip-flops in the TPG *(i.e.* a modified LFSR) during one clock cycle. During the next clock cycle, the second half of the D flip-flops is activated by another clock which speed is also half of the normal speed. The two clocks are synchronous with a master clock *CLK* and a period *2T*, and their phases are shifted by *T*. The master clock *CLK* is the clock of the circuit in the normal mode. The basic scheme of the proposed low power test pattern generator with the corresponding clock waveforms are depicted in Figure 6.

One test vector is applied to the CUT at each clock cycle of the test session, but only one half of the circuit inputs are activated during this time. Consequently, the switching activity in a time interval *(i.e.* the average power) as well as the peak power consumed in the CUT are minimized. Moreover, the power consumed in the TPG is also minimized since only one half of the D flip-flops in the TPG can be activated in a given time interval. Another important feature of the proposed solution is that the total energy consumption during BIST is

reduced since the test length produced by the modified LFSR is roughly the same as the test length produced by a conventional LFSR-based TPG to reach the same or sometimes a better fault coverage.

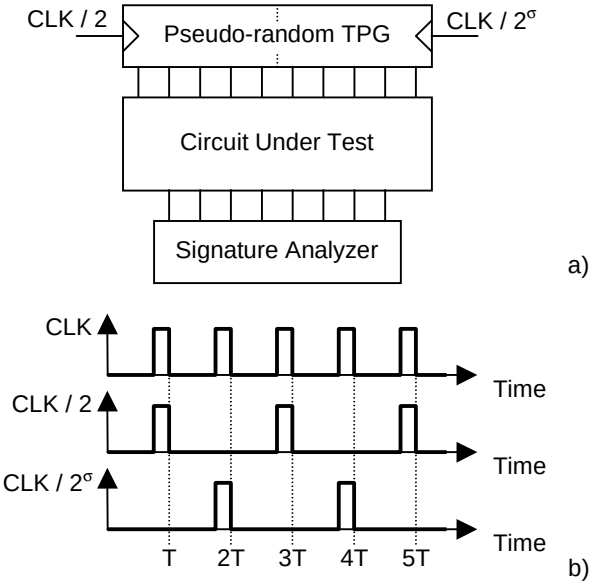

Figure 6: Low power test pattern generator
a) basic scheme and b) waveform of the clock signals

Compared with existing low power BIST techniques, this solution offers a number of advantages. The fault coverage and the test time are roughly the same as those achieved with a standard BIST scheme. The area overhead is negligible and there is no penalty on the circuit delay. The proposed BIST scheme does not require any circuit design modification beyond standard BIST, is very easy to implement and has low impact on the design time. Reductions of the energy, average power and peak power consumption during test operation are up to 94%, 55% and 48% respectively for ISCAS and MCNC circuits.

4. Power conscious functional BIST for the LEON processor

The basic idea consists in using the functional deterministic BIST for microprocessors [Che00]. The main difference to the classic functional processor test is the relation to structural faults and the use of pre-computed deterministic test sets. This kind of solution allows to obtain a high fault coverage while reducing the test time (*i.e.* at speed testing) and the area overhead (*i.e.* functionality reused).

In the followings parts, we present an overview of the processor used (LEON processor [leo01]) as well as a summary of the activities in the field of Low Power Deterministic Functional BIST.

4.1. LEON processor overview

The LEON model implements a 32-bit processor corresponding to the SPARC V8 architecture. It is designed for embedded applications with the following features on-chip:

- separate instruction and data caches,
- hardware multiplier and divider,
- interrupt controller,
- two 24-bit timers,
- two UARTs,
- power-down function,
- watchdog,
- 16-bit I/O port
- and flexible memory controller.

A block diagram of LEON can be seen in Figure 7.

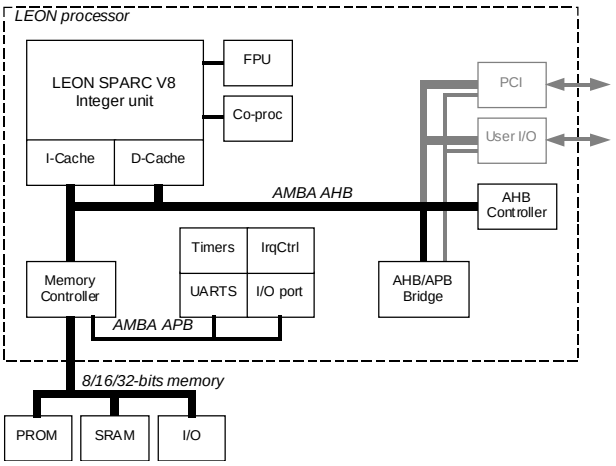

Figure 7: LEON block diagram [Leo01]

4.2. Current work

Existing BIST techniques belong to the class of structural BIST. Structural BIST, such as scan-based BIST techniques, offer good test quality but require addition of dedicated test circuitry (such as full-scan, LFSRs for pattern generation, MISRs for data analysis and test controllers). Therefore, they incur non-trivial area, performance and design time overhead. Moreover, structural BIST applies non-functional, high-switching random patterns and thus, causes much higher power consumption than normal system operations. Also, to apply at-speed tests to detect timing related faults, existing structural BIST needs to resolve various complex timing issues related to multiple clock domains,

multiple frequencies and test clock skews that are unique in the test mode.

While logic BIST may perform well on industrial application specific integrated circuits (ASICs), it is often less feasible for microprocessors. This is because the design changes required for making a microprocessor BIST-ready may come with considerable cost, such as substantial manual effort and significant performance degradation. In addition, microprocessors are especially random pattern-resistant. Due to the timing-critical nature of microprocessors, test points may not be acceptable as a solution to this problem. Even deterministic BIST may lead to unacceptable area overhead, as the size of the on-chip hardware for encoding deterministic test patterns depends on the circuit testability.

All these problems related to the BIST of microprocessor motivate the development of the functional deterministic BIST approach. This time, the test pattern generation is realized with the help of the instruction set of the processor. In fact, most of the time, software instruction have the ability of guiding the test patterns through a complex processor, avoiding the blockage of the test data due to non-functional control signals as in the case of hardware-based logic BIST.

A processor self-test methodology is developed and applied to the Leon processor. It uses random or deterministic patterns, generated directly on-chip. Second, a high fault coverage of manufacturing defects is obtained by targeting structural faults directly, as opposed to functional faults targeted by techniques using random instructions [She98, Bat99]. Third, we propose to use the functionality of the processor, as in [Che00], to generate test patterns on-chip but also to apply the test patterns and to analyze the test responses at the clock speed of the processor.

Investigations with the example of the Leon processor have shown that commercial ATPG tools are not able to perform sequential test pattern generation for this processor as a whole, if a scan path is not included.

Some parts of the LEON processor require very long CPU time (more than one day) in order to generate a deterministic sequence without functional information. In addition, the resulting stuck-at fault coverage stays very low. In fact, most of the time, a standard ATPG generates or tries to generate test patterns for faults that never occur during the standard mode.

By using the instruction set of the processor, test patterns, which are generated just for the hard to test modules, may be driven to the critical parts. Since test mode and system mode are identical in this case, all the power saving means implemented by the system designer can be exploited also for BIST.

This type of approach may be extended to a complete System-on-Chip (SoC) design. In this case, the BIST will reuse the existing test resources (*i.e.* microprocessor). The programmable cores on the SoC (such as processor, DSP and FPGA cores) are used as a pattern generator and response analyzer to test on-chip buses, interfaces between cores or even other cores including digital, mixed-signal and analog components. The microprocessor (core or IP) is programmed in order to run several test programs dedicated to different cores (digital or analog cores) included in the SoC during the test phase. The area overhead of this approach is negligible with regard to classical BIST techniques using additional modules dedicated to the test (*i.e.* LFSR like test pattern generator and signature analyzer), and power dissipation in test mode does not differ much from power dissipation in system mode.

5. Conclusion

In this paper, we discussed what are the important problems for self-testing recent VLSI circuits and systems. These problems directly address the test cost and the power consumption during the test phase. They involve the use of BIST techniques and more especially functional deterministic BIST when complex microprocessors are under consideration. In fact, such a technique offers the advantage not to insert additional blocks dedicated to the test like test pattern generator and signature analyzer. The BIST functions are directly realized by programming the system, deterministic BIST technique for microprocessor and all the means for power awareness put into the system design are also available during testing.

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