

Amlan Ganguly

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Objective

To obtain a research position in the field of Interconnection Infrastructures of Multi-Core Processors/SoCs.

Education

Washington State University, PhD. Electrical and Computer Engineering (August 2010) GPA: 3.89/4.00

Washington State University, M.S. Electrical Engineering (May 2007) GPA: 3.85/4.0

Indian Institute of Technology, Kharagpur, B.Tech (Hons) Electronics and Electrical Communication Engineering; (May 2005) GPA 8.86/10

Professional Experience

- Graduate Student Researcher at the School of Electrical Engineering and Computer Science, Washington State University, Pullman, WA, USA, (January, 2006-present).
- Component Design Engineer at Intel India Development Centre (IIDC), Bangalore, India: Register File Design Team; Whitefield Project. (July 2005-December 2005)
- Internship at Motorola India Pvt. Ltd., Bangalore, India: Developed a novel algorithm for prediction mode selection for Intra-Prediction in an H.264/AVC encoder.

Research Experience

Graduate Research Projects

Architecture space exploration to enhance the performance of NoCs with **wireless interconnects**

- Design of hybrid **Wireless NoC (WiNoC)** with **hierarchical Small-World topologies** with wireless shortcuts.
- Design of efficient communication and routing protocols for such an NoC
- Design of NoC components like **switches** and **Wireless Base Stations (WBs)** for the WiNoCs
- Optimized deployment of wireless transceivers with respect to varying traffic patterns.
- Analysis and minimization of associated overheads for wireless link deployment.
- Use of radiation characteristics of **Carbon Nanotube (CNT)** structures to create miniaturized antennas.
- Use of appropriate modulation methodology to boost power, range and channel width of CNT-based antenna structures.

Characterization and comparative analysis of emerging interconnect technologies

- Perform a comparative study of all radical interconnect technologies in light of how these can revolutionize NoC research.
- Compare alternatives and establish benchmarks with various parameters like system size and traffic patterns.
- Present conclusive arguments for choice of best technology for particular environments.

Implementation of WiNoC architectures with mm-wave antennas

- Design of WiNoC architectures employing mm-wave transceivers as a more near-term alternative with readily CMOS process compatibility
- Design of proper routing protocols with mm-wave characteristics
- Characterize performance profiles of such WiNoCs

Development of Fault-Tolerant Interconnection infrastructure for Multi-Processor SoC Platforms

- Developed and implemented novel **coding schemes** in NoC switches to enhance transient error resilience in MP-SoC or NoC interconnect fabrics.
- Design and modification of NoC switches to create **fault-tolerant and robust** on-chip interconnection network.
- Implementation of Crosstalk Avoidance Codes and comparison against traditional techniques like shielding and spacing.
- Implementation of Joint Crosstalk Avoidance and Single Error Correction Codes as a part of NoC switches using a unified framework for low-power, crosstalk avoidance and error resilient coding.
- Development of a joint Crosstalk Avoidance and Double Error Correction scheme called **CADEC**. Able to achieve lower energy dissipation compared all similar error correcting schemes in literature.
- Development of a joint Crosstalk Avoidance and Multiple Error Correction scheme called Joint Crosstalk Avoidance and Triple Error Correction Code (**JTEC**) and Simultaneous Triple Error Correction and Quadruple Error Detection Code (**JTEC-SQED**) capable of correcting higher number of errors and reduce energy dissipation in communication across the NoC fabric.
- Implementation of such error recovery schemes in the **wireless NoC** fabrics and NoCs with other emerging interconnection technologies as they are inherently more prone to defects and random errors

Clock Domain Synchronization in big Multiprocessor SoCs

- Finding **optimum number of clock domains** to minimize synchronization energy
- Placement and layout of individual clock domains to optimize energy dissipation

Undergraduate Research Projects

Design of a Novel Pollution Control mechanism for Automobiles

- Using DIP controller to control excessive fuel injection into the combustion chamber.
- The work was done as collaboration between Indian Institute of Technology, Kharagpur and University of Trento, Italy.

Design of a Novel Algorithm for reducing Spatial Redundancy in the H.264/AVC code

- Using a threshold based technique to select intra-prediction mode to recreate images in the H.264 standard.

Technical Skills

- Hardware Description Languages: Extensive coding in VHDL and Verilog.
- Tools Used:
 - 1) Synopsys
 - Design Analyzer, PrimeTime, PrimePower, HSpice, TetraMAX ATPG
 - 2) Cadence
 - Spectre, Virtuoso
 - 3) Xilinx.
- Xtensa Toolsets

- Extensive programming experience with C/C++, MATLAB, SIMULINK, Assembly Language (Intel 80x86 and MIPS)
- Operating System: WINDOWS and LINUX/UNIX.
- Others: Microsoft Office Suite.

Publications

Book Chapters:

1. Partha Pratim Pande, Cristian Grecu, **Amlan Ganguly**, Andre Ivanov, and Resve Saleh, "Test and Fault Tolerance of NoC Infrastructures", In *Networks-on-Chips: Theory and Practice*, Fayez Gebali, Haytham Elmiligi, and M.Watheq El-Kharashi (eds.), Taylor & Francis Group LLC - CRC Press.

Journals:

1. **Amlan Ganguly**, Partha Pande, Benjamin Belzer, "On the Role of Error Control Coding in Enhancing Reliability of a Wireless Network-on-Chip", *IEEE Design and Test of Computers, (D&T) under preparation*.
2. Sujay Deb, Kevin Chang, **Amlan Ganguly**, Xinmin Yu, Partha Pande, Deuk Heo, Benjamin Belzer, "Network-on-Chip Architectures With mm-wave Wireless Interconnects", *IEEE Transactions on VLSI (TVLSI), under preparation*.
3. **Amlan Ganguly**, Kevin Chang, Sujay Deb, Partha Pande, Benjamin Belzer, Christof Teuscher, "Scalable Hybrid Wireless Network-on-Chip Architectures for Multi-Core Systems", *IEEE Transactions on Computers (TC)*, August, 2010, URL: <http://www.computer.org/portal/web/csdl/doi/10.1109/TC.2010.176>
4. **Amlan Ganguly**, Partha Pande, Benjamin Belzer, "Crosstalk-Aware Channel Coding Schemes for Energy Efficient and Reliable NoC Interconnects", *IEEE Transactions on VLSI (TVLSI)* Vol. 17, No.11, November 2009, pp. 1626-1639.
5. **Amlan Ganguly**, Partha Pande, Benjamin Belzer, Cristian Grecu, "Design of Low power & Reliable Networks on Chip through joint Crosstalk Avoidance and Multiple Error Correction Coding", *Journal of Electronic Testing: Theory and Applications (JETTA)*, Special Issue on Defect and Fault Tolerance, June 2008, pp. 67-81.
6. Partha Pande, **Amlan Ganguly**, Haibo Zhu, Cristian Grecu, "Energy Reduction through Crosstalk Avoidance Coding in Networks on Chip", *Journal of System Architecture (JSA)*, Vol. 54/ 3-4, March-April 2008, pp.441-451.

Conferences:

1. Sujay Deb, Kevin Chang, **Amlan Ganguly** and Partha Pande, "Comparative Performance Evaluation of Wireless and Optical NoC Architectures", *Proceedings of IEEE International SOC Conference (SOCC)*, 27th-29th September 2010.
2. Sujay Deb, **Amlan Ganguly**, Kevin Chang, Benjamin Belzer, Deuk Heo, "Enhancing Performance of Network-on-Chip Architectures with Millimeter-Wave Wireless Interconnects", *Proceedings of IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, 2010.

3. Partha Pande, **Amlan Ganguly**, Kevin Chang, Christof Teuscher, "Hybrid Wireless Network-on-Chip: A New Paradigm in Multi-Core Design", *invited paper*, Second International Workshop on Network-on-Chip Architectures (**NoCArc**), December 12, 2009.
4. **Amlan Ganguly**, Kevin Chang, Partha Pratim Pande, Benjamin Belzer and Alireza Nojeh, "Performance Evaluation of Wireless Networks on Chip Architectures", Proceedings of the IEEE International Symposium on Quality Electronic Design (**ISQED**), 16th-18th March 2009.
5. Partha Pande, **Amlan Ganguly**, Benjamin Belzer, Alireza Nojeh, Andre Ivanov, "Novel Interconnect Infrastructures for Massive Multicore Chips", Proceedings of IEEE Symposium on Circuits and Systems (**ISCAS**), May, 2008, pp. 2777 - 2780.
6. A. Nojeh, P. Pande, **A. Ganguly**, S. Sheikhaei, B. Belzer and A. Ivanov, "Reliability of wireless on-chip interconnects based on carbon nanotube antennas," Proceedings of IEEE International Mixed-Signals, Sensors, and Systems Test Workshop (**IMS3TW**) June 2008, pp. 1-6.
7. **Amlan Ganguly**, Partha Pande, Benjamin Belzer, Cristian Grecu, "Addressing Signal Integrity in Networks on Chip Interconnects through Crosstalk-Aware Double Error Correction Coding", Proceedings of IEEE Computer Society Annual Symposium on VLSI (**ISVLSI**) 2007, May, 2007, pp. 317 - 324.
8. Partha Pande, **Amlan Ganguly**, Brett Feero, Cristian Grecu, "Applicability of Energy Efficient Coding Methodology to Address Signal Integrity in 3D NoC Fabrics", Proceedings of IEEE International ON-line Test Symposium (**IOLTS**), July, 2007, pp. 161-166.
9. Partha Pande, **Amlan Ganguly**, Brett Feero, Benjamin Belzer, Cristian Grecu, "Design of Low Lower & Reliable Networks on Chip through Joint Crosstalk Avoidance and Forward Error Correction Coding", Proceedings of IEEE Defect and Fault Tolerance in VLSI Systems (**DFT**), 2006, pp. 466 – 476.
10. Partha Pande, Haibo Zhu, **Amlan Ganguly**, Cristian Grecu, "Energy Reduction through Crosstalk Avoidance Coding in NoC Paradigm", Proceedings of IEEE EUROMICRO Conference on Digital System Design: Architectures, Methods and Tools (**DSD**) 2006, pp. 689 – 695.
11. Partha Pratim Pande, Haibo Zhu, **Amlan Ganguly**, Cristian Grecu, "Crosstalk-aware Energy Reduction in NoC Communication Fabrics", Proceedings of IEEE International SOC Conference (**SOCC**), 2006, pp. 225 – 228.
12. Shantiram Kal, **Amlan Ganguly**, Andrea Boni, "An embedded system for pollution control in automobiles by using a MEMS accelerometer signal", Proceedings of IEEE Conference on Emerging Technologies and Factory Automation (**ETFA**) Sept. 2005, pp. 733-739.

Teaching Experience

Instructor for

- EE466: VLSI Design (URL: <http://eecs.wsu.edu/~ee466/>)

Teaching Assistant for the following courses

- ASIC and Digital Systems Design
- VLSI System Design
- Electrical Circuits and Systems
- Analog Laboratory Course
- Renewable Energy Sources

Honors and Awards

- Outstanding PhD Student Award in Computer Engineering, School of EECS, WSU, 2010.
- Winner of Travel Grant from WSU to present a publication at ISQED, March 2009, at San Jose, California.
- Winner of Travel Grant from IEEE, ISCAS, 2008.
- Outstanding Masters Student Award, School of EECS, WSU, 2007.
- Winner of Travel Grant from WSU to present a publication at ISVLSI, May 2007, at Porto Alegre, Brazil.
- 1600/1600 General GRE score.
- Ranked 297 in IIT-JEE examination (in the top 0.2% among 150000 candidates nationwide).
- Awardee of the Jagadis Bose National Science Talent Search Scholarship (JBNSTS), a nationwide contest among college freshman students.

Extra Academic Activities

- President of the India Student Association, Pullman Washington, July 2006-May 2007.
- Won several Quiz and Debate competitions at school level.
- Member of the IIT Dramatics team.

Referees

1. Dr. **Partha Pratim Pande**, Asst. Professor, School of Electrical Engineering & Computer Science, Washington State University, PO BOX 642752 Pullman, Washington 99164-2752, Phone 509-335-5223, Fax 509-335-3818, email: pande@eecs.wsu.edu
2. Dr. **Benjamin Belzer**, Associate Professor, School of Electrical Engineering and Computer Science, Washington State University, PO BOX 642752 Pullman, Washington 99164-2752, Phone 509-335-4970, Fax 509-335-3818, email: belzer@eecs.wsu.edu
3. Dr. **Christof Teuscher**, Assistant Professor, Electrical and Computer Engineering, Portland State University, FAB 20-13, ECE Department Portland State University Post Office Box 751 Portland, OR 97207-0751, Phone: 503.725.2817, teuscher@pdx.edu
4. Dr. **Deuk Heo**, Assistant Professor, School of Electrical Engineering and Computer Science, Washington State University, PO BOX 642752 Pullman, Washington 99164-2752, Phone 509-335-1302, Fax 509-335-3818, email: dheo@eecs.wsu.edu
5. Dr. **Alireza Nojeh**, Assistant Professor, Electrical and Computer Engineering, The University of British Columbia, Kaiser 4041, 2332 Main Mall, Vancouver, BC, Canada V6T 1Z4, Tel: + 604 827 4346, Fax: + 604 822 5949, email: anojeh@ece.ubc.ca