A DYNAMIC CONTENT ADDRESSABLE MEMORY USING A 4-TRANSISTOR CELL

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Abstract

A novel ternary dynamic content addressable memory cell with coupled match lines is presented here. The dynamic CAM cell contains only four n-type transistors. This cell is capable of storing and matching three states, hence the term ternary; these states are: zero (0), one (1) and don't care (X). Circuit simulations show that our dynamic CAM cell performs all the basic operations (read, write and match) at a good speed. In order to use the proposed cell in a CAM array, we developed a cut-off scheme to deal with coupling.

1 Introduction

A content addressable memory (CAM) allows access to memory on the basis of data values rather than addresses. It also allows for parallel data comparisons. A CAM compares input data with stored data; if the input data matches the stored data, this indicates that a matching condition exists in the CAM [1]. Thus, matching involves comparing presented data to the stored data, and the results of a match search are determined by the status of a match line. The ability to store a don't care (X) in a ternary CAM cell gives the ternary CAM its major advantage over a binary CAM for a number of applications.

Other CAM's basic operations are write and read. The write function enables data to be stored into the CAM, while the read function enables stored data to be retrieved. A single ternary digit or trit constitutes of 0, 1 and X (don't care). Ternary CAMs find applications in logical inferencing, pattern-matching and in applications that require searches in specified address ranges.

This paper has been organized as follows. Section 2 of this paper describes a dynamic content addressable memory (DCAM) cell, and its operation. In Section 3 the dynamic CAM is incorporated onto an array, we describe here the coupling problem and a solution to it. In Section 4 we provide some concluding remarks.

2 4-T dynamic CAM cell

In this section we present a four-transistor dynamic content addressable memory cell. The dynamic CAM cell is designed to store a ternary digit per comparison bit [2], [3]. The match line for this cell is coupled with one of the cell's transistor. The three basic operations that need be performed by the DCAM cell are: match, write, and read.

The four-transistor (4-T) dynamic content addressable memory (DCAM) cell, shown in Figure 1, consists of exclusively n-type transistors. This cell has two transistors (T_{c1} and T_{c0}) arranged in an exclusive-OR configuration in order to perform a comparison between the data presented at the BIT and NBIT lines and data stored in the cell. The gates of these transistors serve as dynamic data storage elements; these nodes are labeled $Sb1$ and $Sb0$. Transistors T_{w1} and T_{w0} are used to write into these nodes $Sb1$ and $Sb0$. When transistors T_{w1} and T_{w0} are conducting, data on the bit lines (BIT and NBIT) gets transferred to locations $Sb1$ and $Sb0$. Turning off transistors T_{w1} and T_{w0} isolates the dynamic storage elements from the bit lines.

The DCAM cell is designed to store three states, namely don't care (X), one (1) and zero (0). These three states are set by $Sb1$ and $Sb0$. Table 1 shows how the three states are stored in the dynamic CAM cell.

Table 1: DCAM cell stored states.

$Sb1$	$Sb0$	state
0	0	X (don't care
0	1	0 (zero)
1	0	1 (one)
1	1	not allowed

2.1 Match operation

The match line is directly connected to the exclusive-OR (XOR) output; thus, the state of this line depends on the XOR output. This XOR is formed

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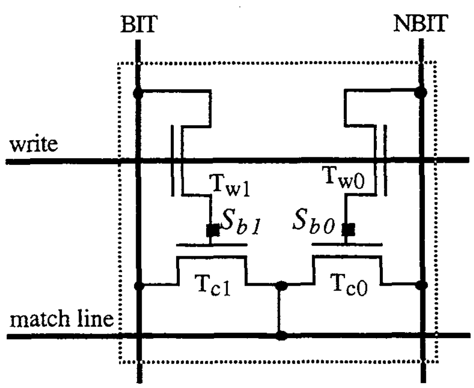

Figure 1: 4-T DCAM cell.

by transistors T_{c1} and T_{c0}. If the XOR output is at logic level "1", the match line will not be discharged, indicating that a match has been found. On the other hand, if the XOR output is at logic level "0", the match line gets discharged, indicating a non-matching condition.

The matching operation for the DCAM cell involves comparing the data presented on the bit lines (BIT and NBIT lines) to the stored data, and evaluating the match line. The match line is precharged to logic level 1 before comparing the stored data with the input. This is done by means of the transistor T_{pcg} which is set active by the signal precharge; this transistor is shown in Figure 2. It should be pointed out that this transistor precharges the match line which is shared by all CAM cells in the same row.

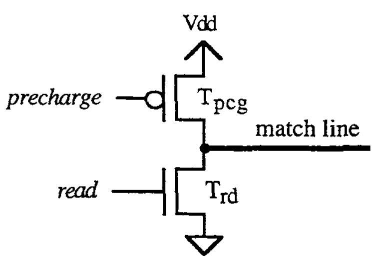

Figure 2: Match line's precharge and read signals.

Since the output of the XOR is connected to match line, when there is a mismatch between the stored data and the input, the XOR output is set to logic "0". This in turn discharges the match line. If a match is found, the exclusive-OR output is "1"; thus, there is no discharge of the match line.

If a don't care state exists in the DCAM, any input presented on the bit lines will result in a matching condition. When zeros are stored at $Sb1$ and $Sb0$, transistors T_{c1} and T_{c0} are always off, preventing data from either the BIT or the NBIT line to be passed to the match line. Matching and non-matching conditions along with the corresponding status of the bit lines are summarized in Table 2. A non-matching condition will occur whenever the data on the bit lines is not the same as the stored data in the CAM cell. A "1" on the match line indicates that a match has been found, while a "0" indicates a non-matching condition.

Table 2: Table for the match operation.

stored data	$Sb1$	$Sb0$	BIT	NBIT	match condition
0	0	1	0	1	match
0	0	1	1	0	no match
1	1	0	1	0	match
1	1	0	0	1	no match
X	0	0	X	X	match

2.2 Write and read operations

The other two CAM's basic operations (write and read) are described in this subsection. The write operation is performed by explicitly setting transistors T_{w1} and T_{w0} in a conducting mode by having the write line signal at logic "1". Data at BIT and NBIT lines is transferred to the gates of transistors T_{c1} and T_{c0}, respectively. The write line is common to all the CAM cells in the same row. It should be pointed out when a write operation is taking place, the match line should be kept floating (i.e. the transistors T_{pcg} and T_{rd} are set off). This is necessary to ensure that the proper voltage level is stored. This is of particular importance when a logic 1 is stored, since this data makes the transistor to conduct and a connection between one of the bit lines and the match line exists.

The read operation requires a bit more elaborated scheme. This operation requires that BIT, NBIT and match lines be precharged to a logic 1. Once these lines are precharged, reading takes place by setting the read signal to high; this in turn makes the transistor T_{rd} active setting the match line to ground (see Figure 2). If a "1" is stored in either $Sb1$ or $Sb0$, the match line (by means of transistor T_{rd}) discharges BIT or NBIT lines. On the other hand if either (or both in the case of a don't care state) $Sb1$ or $Sb0$ has a "0" the lines are not discharged. Thus, what is read onto BIT and NBIT is the inverted signal of what is stored in the CAM cell.

The read and write operations, when combined, constitute a refresh operation that is needed for dynamic cells such as the proposed CAM cell.

3 CAM array

In this section we present the design of an array having the 4-transistor CAM as the basic cell. As mentioned earlier, cells in the same row share write and match lines while cells in the same column share the same BIT and NBIT lines. Forming an array is straight forward, since the same cell is replicated as many times as required by the array size.

3.1 Matching on a CAM array

It is important to study the matching function since this is the main operation that a CAM array performs. Figure 3 shows a 2×2 piece of an array with an example of a matching operation. In this example the row i matches the input thus match line i should remain at logic (since it has been precharged). Next row (i+1) has a no match condition. Cell $CAM_{i+1,j+1}$ has a mismatch where the input is "0" and what is stored is a "1". The "0" at BIT_{j+1} causes the match line i+1 to be discharged. The transistor (connected to BIT_j line) at cell $CAM_{i,j+1}$ has a "1" at its gate; thus, this transistor is conducting. Due to coupling, this transistor has on one side the match line i+1 which is discharged and at the other end the BIT_j line which has a "1". This path shown in Figure 3 is formed of n-type transistors; this in turn provides a better path for transmitting voltages closer to zero than to V_{dd} (5V in this case). This path is formed when matching occurs and affects other match lines including the one(s) that would match.

A Spice simulation that shows the effects of coupling on the match lines is plotted in Figure 4. The non-matching signal falls down towards zero as it is expected, and the matching signal falls down as well. However, it can be observed that the matching signal has a delay and a less sharp slope. This is due to the fact that the non-matching line needs to be discharged before it can affect a matching line. The influence of the non-matching line over the matching line is mitigated by the BIT (or NBIT) line driver. These features can be used to design a CAM array that performs matching in a reliable manner.

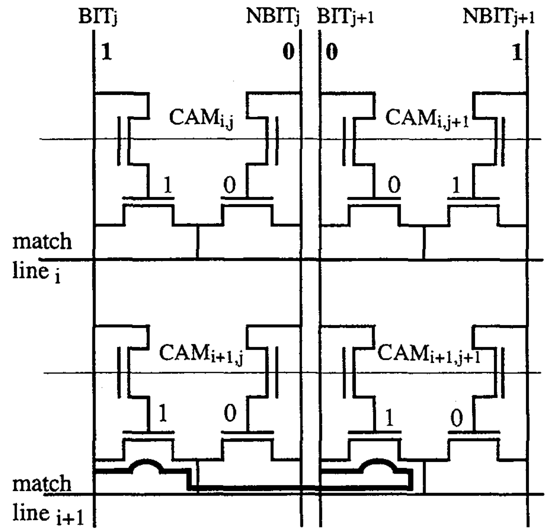

Figure 3: 2×2 CAM array.

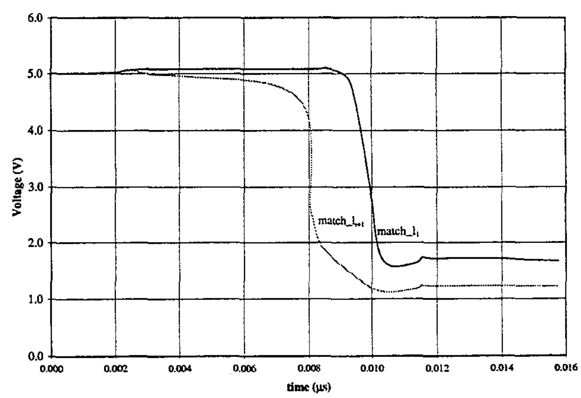

Figure 4: Coupling effects on the match lines.

3.2 Cut-off scheme

In order to deal with coupling effects on the match lines, we have devised a simple match line cut-off scheme. Figure 5 shows the scheme where the match lines from the array are allowed to pass on to a set of inverters until all the non-matching signals have reached a value considered as logic "0". Once all the non-matching signals have produced a "0", the pass transistors are put into the cut-off region. This in turn prevents any further discharge of the match line and, therefore, the matching condition(s) is (are) preserved. In order to accomplish this, we have included a circuit that reproduces the worst non-matching time. This circuit is just a row of CAM cells with a non-matching condition that needs a relatively long time to obtain. This signal is used as cut-off signal for the gate of the transistors labeled as T_{cf}. This signal as mentioned earlier follows the worst case non-matching condition time. The cut-off signal must come before any matching condition falls down to a logic "0" status. The set of inverters at the end of the match line signals does not represent extra hardware since these are used to buffer the signals for most of the dynamic CAM arrays [4], [2], [5].

A Spice simulation of a 8×8 array is presented in

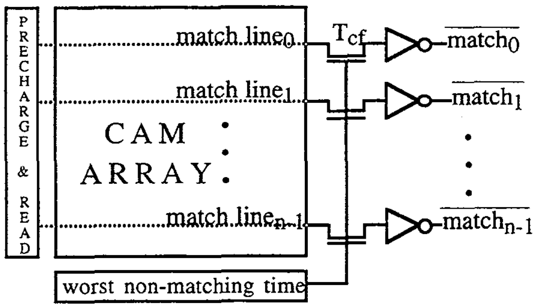

Figure 5: CAM array with a match line cut-off scheme.

Figure 6. It can be observed that the match outputs of the non-matching signals (1, 3 and 8) go to 5 volts while the matching signal (2) remains at voltage close to 0V. In this plot the cut-off signal (labeled as control signal) is also included which is the last to come down before the matching signal comes down. It should be noticed that the cut-off signal allows enough time for all the non-matching conditions to reach a level below 2V. At 2V the signals are considered as logic 0, and the inverters are triggered producing the outputs shown in the figure.

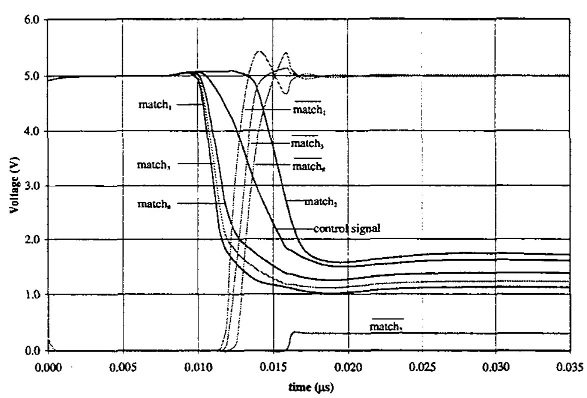

Figure 6: Match lines and match output on a 8 × 8 array.

4 Concluding remarks

In this paper we have presented a novel dynamic CAM cell that utilizes only 4 n-type transistors. We have described its major features, implementation issues, and system integration. This cell performs the required functions: match, read, and write. Due to coupling, the match line is affected by non-matching conditions. However, we have shown that by using a cut-off scheme this problem can be overcome. The proposed cell can be a good candidate for CAM applications that require minimum silicon area.

References

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