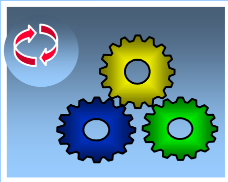
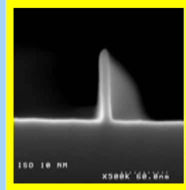
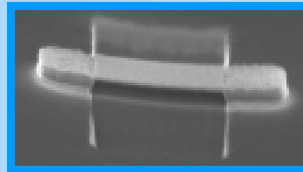
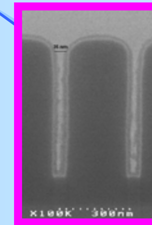
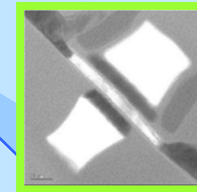
Overview of Nanotec 300 program



Leti missions and positioning in core CMOS technology

Nanotec spirit and structuring models

The operational context

The competence centers

Nanotec roadmaps

Leading projects

European vision

Marie-Noëlle Séméria

mnsemeria@cea.fr

3 axes of development in microelectronics and in Leti activity

bipolar
rf
MEMS
power source
biochips

diversification

130nm
90nm
65nm
45nm
32nm
22nm

scaling

BiCMOS
rf CMOS + passives
embedded MEMS
environnement conscious smart devices
FD SOI
Multi Gate CMOS

dedicated markets

Where cultures meet and imagination creates

Moore's law

300mm

innovation from nanosciences

Leti missions in core CMOS technology

- 65nm : Technological support and expertise
- 45nm : Path finding and partial integration
  - Technological compatibility
  - Alignment with ITRS and industrial roadmap (GP,LP, HP)
- 32 nm and beyond : Early development
  - Prove of concept at the right Lg and directions
  - knowledge of roadblocks

    Simulation, modeling and design

    Characterization

    Architecture

    Technological modules

Leti global positioning in core CMOS technology

University, CNRS , INPG , CEA - DSM labs

Strong links with academic teams

Basic research reservoir

22nm

exploratory research

CEA - LETI

45 – 32 – 22 nm

Core CMOS technology

Advanced materials and modules development

300mm platform

- focus on critical developments not directly manageable by Crolles 2
- with the best existing tools or future tools (JDP with process equipment, material, characterization tool suppliers)

Alliance – Crolles 2

STM - Freescale- Philips

65 – 45 nm

Common program

Common teams

Coherent strategy of equipments

300mm pilote line

- Base wafers & moves allocation

Multidisciplinary platforms : **bio; opto; molecular**…

An interactive model

Advanced CMOS Platform

N+2, N+3

technological nodes

N+4 and beyond technological nodes

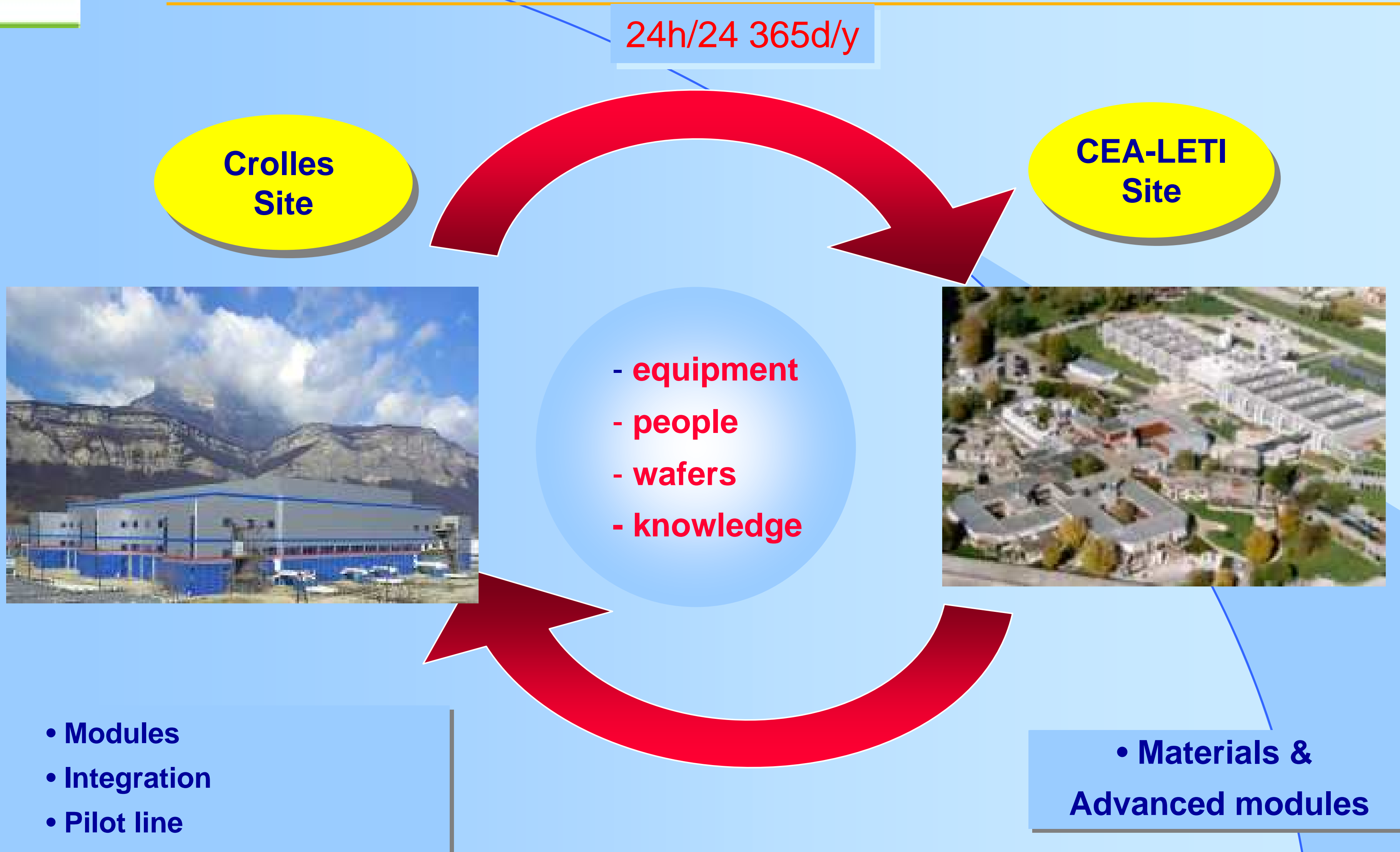
IC Industry

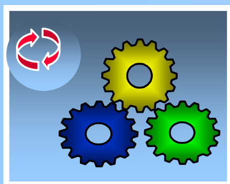
Scientific community

Based on the driving force of partnership

and on the specific features of each partner

The short loop model





The operational context

Nanotec 300 - Leti - Minatec

Crolles

CEA Grenoble site

New clean rooms in existing Building 41 (2003-2005)

Reserved location for a new 300mm building (2006)

Nanotec 300

Leti

Minatec

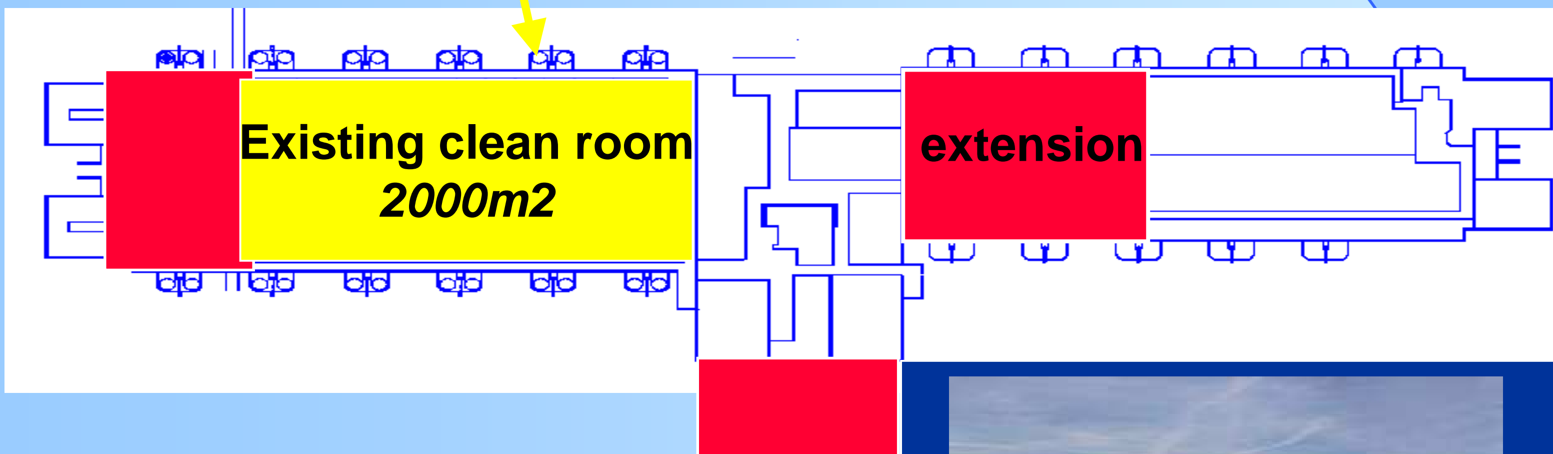
Nanotec 300 - clean room 300mm

1500 m2

300mm clean room

more today

The inauguration day with the Alliance April 22, 2004

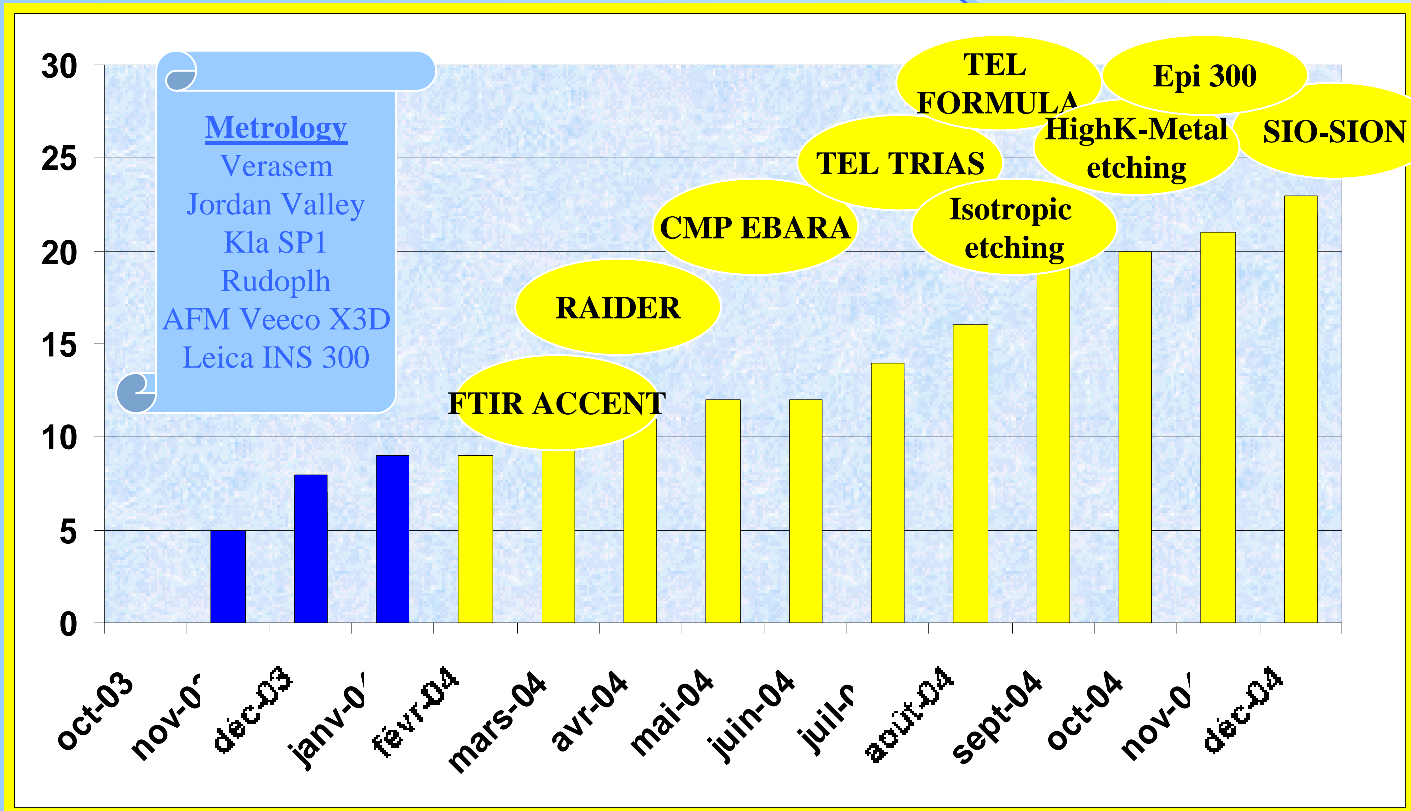


And room for a new connected building (2006)

300mm equipments ramp up

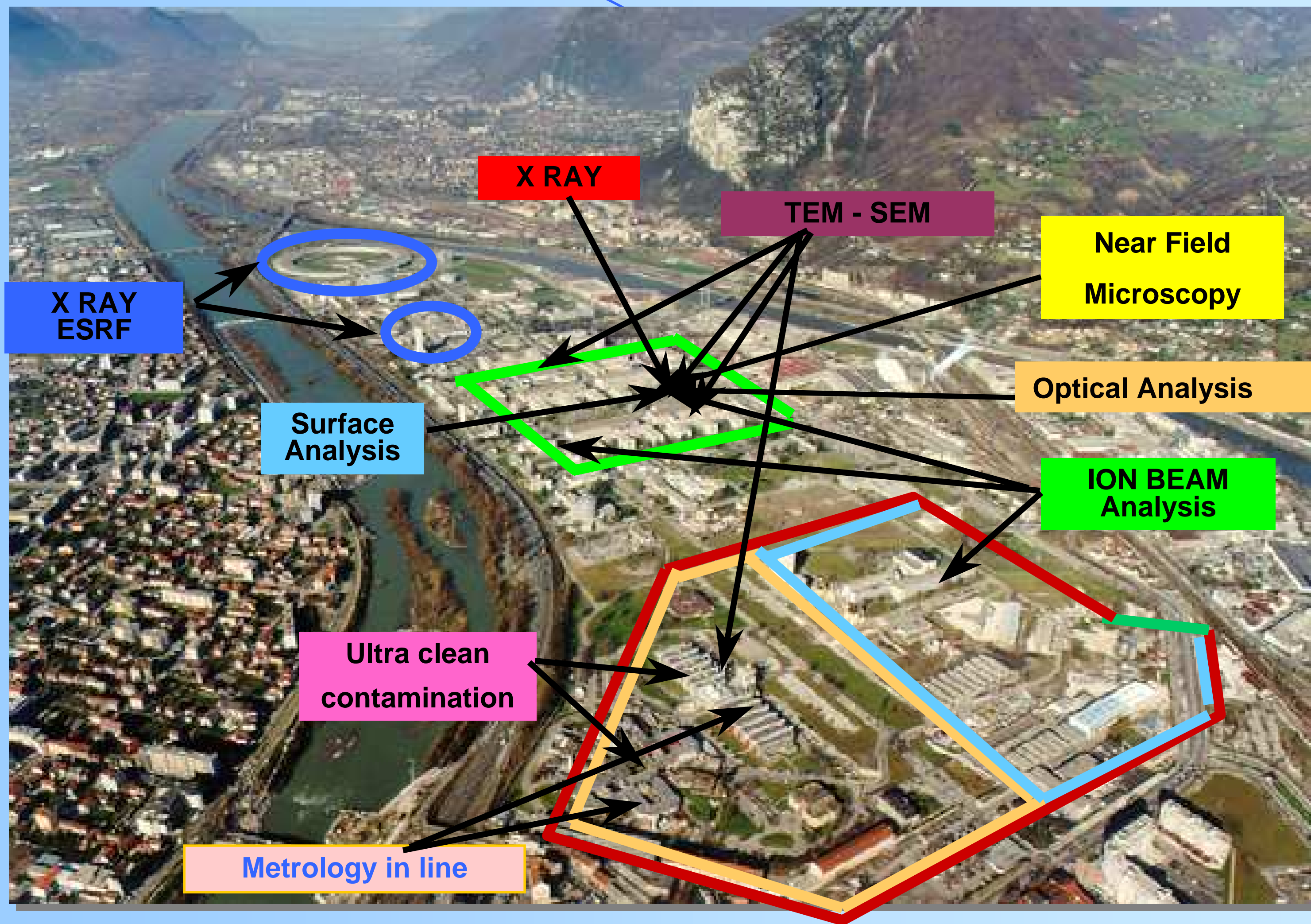
Priority 2003 : metrology

2004 : Front End



Date of delivery

All the characterization on site



3 snapshots on characterization

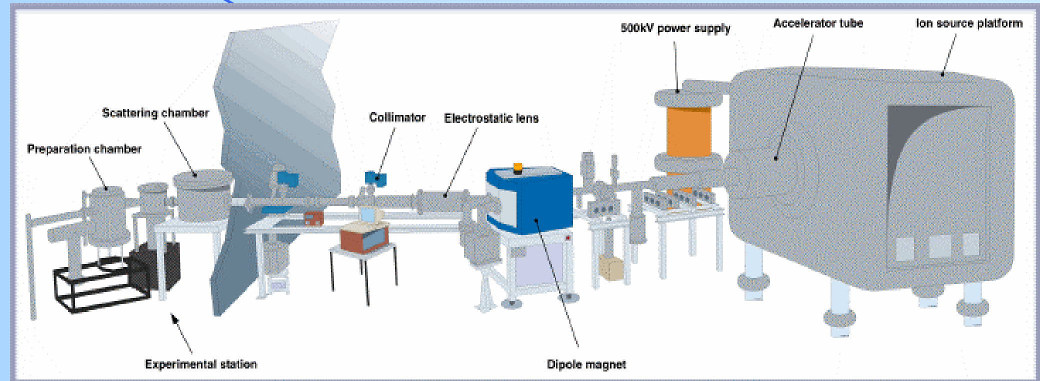
Medium Energy Ion Scattering (MEIS) – Q3 04

Thin films : 0.1nm (RBS 20nm)

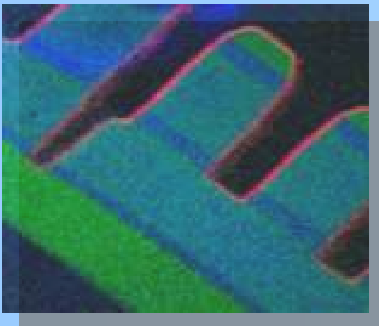
Quantitative composition

Depth profiling

Gate stack, High K & ULK dielectrics



Transmission Electron Microscopy



Sample preparation :
Ion milling Tripod, FIB

TEM-EELS : chemical analysis of interconnects Ti – C - O

TOF SIMS - 2005

Rz : 1nm, Rxy:50nm

Localization

All the elements

insulator

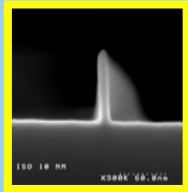
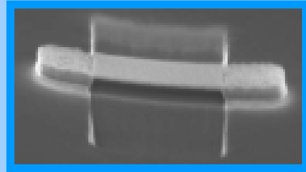
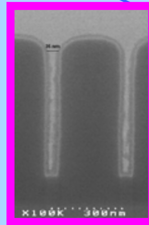
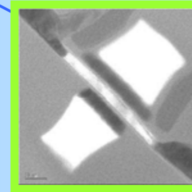
Nanotec 300 : the operational context

A collaboration based on “Competence centers”

- Advanced Lithography
- Front End Materials & Process steps
- Advanced devices
- Back End Materials & process steps
- Modeling/Simulation & Electrical characterization

And benefiting from other large LETI projects…

- Substrate development (common lab Soitec-CEA)
- Growth of the nano-characterization pole (Minatec, Internal LETI Basic Research Program)
- Closer coupling with upstream research (CNRS/LTM hosting, Internal LETI Basic Research Program …)

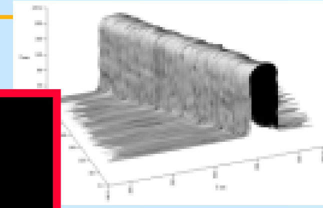





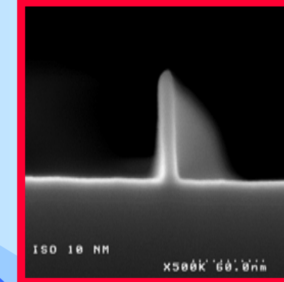
The competence centers

Nanotec roadmaps

Leading projects

Lithography competence center

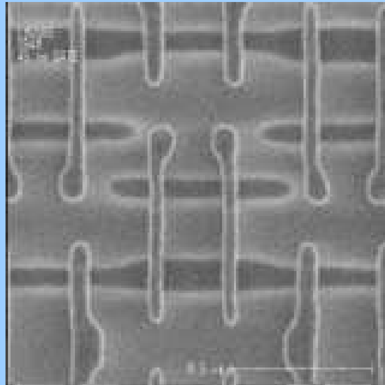




- Optical lithography (248, 193, 193i nm)
  - *Multi sites, interferometric bench*
- EUV
  - *Reflective mask, resist, experimental exposure tool*
- E beam
  - *shaped beam, high resolution, multi beams*
- Nanoimprint
  - *full wafer, stamp and repeat*
- Resist excellence center
  - *understand resist chemistry limitations, support litho cells, anticipate new resists*

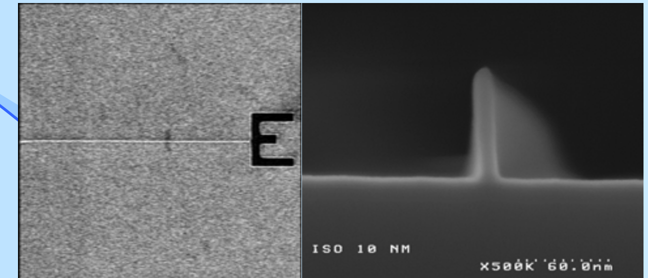
Lithography highlights

e-beam lithography



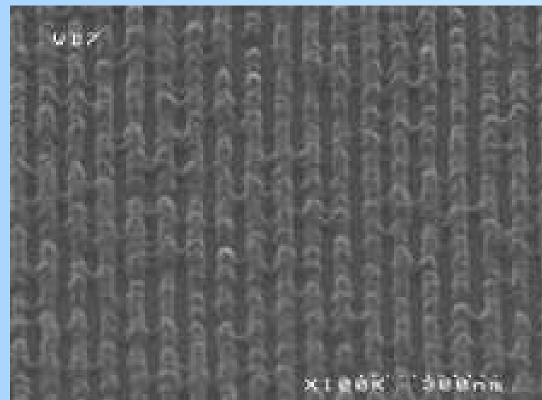
GATE (target : 45 nm pitch 180 nm)

10nm line



e-beam lithography for 65nm SRAM (on Crolles site) – 45nm SRAM in progress

EUV



First EUV exposures (at PSI)

with high resolution

(35 nm dense lines)

Metrology

Scatterometry : algorithm transfer to equipment supplier

Resist/polymer Center

Equipments set-up

Lithography roadmap

	65 nm	45nm	≤ 32nm	Metrology characterization
DUV 193 nm	193nm	immersion 193nm Resist trimming		
Mask less : E beam Variable Shaped Beam High resolution	Process modules develop[t], Devices develop[t] CD ≤45nm Advanced prototyping	CD: 20nm Chemically Amplified resist	CD: 3 – 5 nm Inorganic resist	Scatterometry AFM3D CD-SEM ULV
EUV 13.5nm		Mask – defect metrology Experimental Tool 10X : BEL Resist		
Nano-imprint		CD :20nm Mold, resist For 1 level		
Resist expertise center	Chemical/Physical Characterization Characterization tools development CAR limitations : res. Limit, LER, Pattern collapse, defectivity,.. New material development			

Front End competence center

- High K dielectric

  Hf silicate, process induced damage, high K for eDRAM, high K for NVM, alternative dielectric

- Metal gates

  P+ / N+ materials, ToSi gates, gate stack etching

- Strained Si

  starting materials, epitaxy

- Source, Drain

  NiSi, NiSiGe, NiGe, SPE, laser anneal…

- Technological modules development for each integration

  cleaning, selective etch, CMP, raised S/D…

Front End materials and processing roadmap

	65 nm	45nm	≤ 32nm	Characterization / Simulation
Starting materials		sSiOI, SiGeOI	GeOI, New developments	Defect characterization
Strained layers	Strained SiGe:C on bulk	Strained Si / relaxed SiGe; Strained Si On Insulator		Raman UV Simulation of strain Electrical study : Tstability…
Gate stack	Hf based HiK / Poly Si, SiGe gate	Hf based HiK / Metal gate (WF, TOSI)	Alternative HiK / Metal gate Multi gate architecture	MIR, TXRF, XRR, MEIS,… Electrical study : PID, mobility, Phim pinning
	Surface chemical engineering			
Source, Drain	Solid Phase Epi Flash anneal	Selective epi SiGe, Ge Plasma doping Flash anneal	Low R S,D Plasma doping laser anneal	2D dopant profiling
Etch, strip, clean, CMP, STI	Development for each integration technology			

Strained FD SOI CMOS related projects

National projects
IST projects
MEDEA projects

	2003	2004	2005	2006	2007	Description
Substrate-strain						
RMNT Smarstrain	National	National				New substrate :Strained Si on Insulator, Strained Si on SiGe on insulator
RMNT Stressnet	National	National	National			Understanding stress in IC
MEDEA Silonis			MEDEA	MEDEA	MEDEA	Industrial route of strained SOI substrates fabrication for sub 65nm high performance application
Modules integration & Devices						
MEDEA T206	MEDEA	MEDEA	MEDEA			SOI CMOS LP RF 90 – 65 nm
IST NanoCMOS		IST	IST	IST	IST	45nm HK/Metal gate, Raised S/D,
MEDEA 45nm				MEDEA	MEDEA	

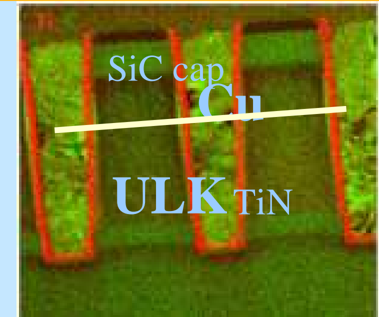
Back End competence center

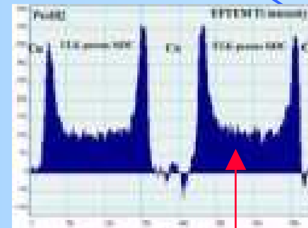
- ULK dielectric
  - *porous materials, ellipsometric porosimetry*
- Air gap
  - *solid first approach*
- Metallic barriers
  - *ALD, ternary barriers electro less deposition, electro grafting*
- Conductors
  - *Cu deposition, seed layers, scaling*
- CMP
- Reliability
  - *electromigration in SD lines (mechanical stress, barriers, Cu filling), dielectric reliability*
- Technological modules development for each integration
  - *cleaning, etch, strip,CMP*

Back End Materials & Processing – highlights

Porous ULK materials

Pore sealing

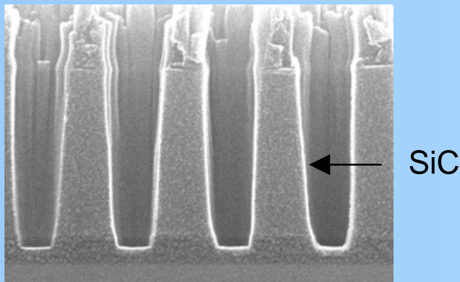




TiN diffused in ULK

Large Reduction of TiN in ULK

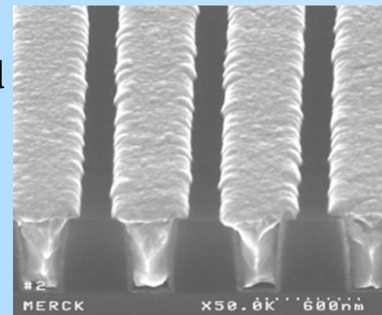
SiC low k dielectric barriers



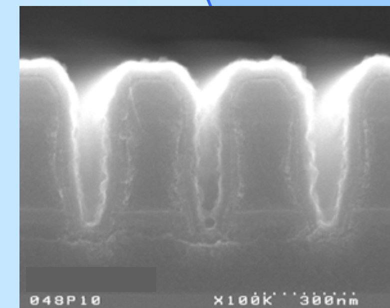
SiC barrier efficiency as etch stopper during the ULK etch : SiOC/SiC selectivity = 24

Metal deposition

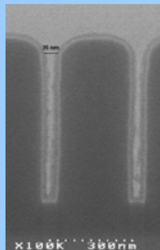
Self aligned NiMoP barriers



Cu « Seed layer » by electrografting



Scaling



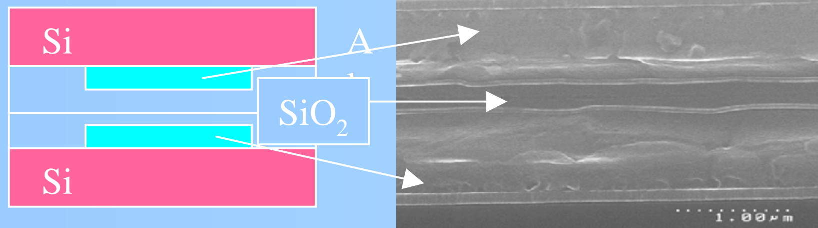
TEM along line length

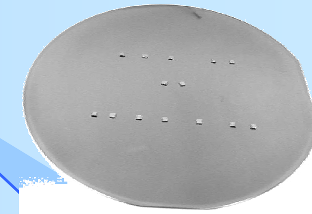
Interconnect roadmap

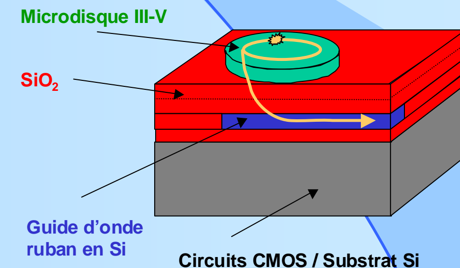
	65 nm	45nm	32nm	Characterization / Simulation
ULK : CVD, Spin on	CVD k=2.4	Porogen Solid First k= 2.2	Spin on Dielectrics Post treatment cure (Ebeam, SCCO2) Post integration porosity approach Advanced precursor Air gap	Ellipsometric Porosimetry FTIR, ATR, AFM, FSM Scatterometry XPS
Conductor	ECMD Cu	Cu ECD seed repair- seed less Metal filling of narrow structures		
Barrier/ Nucleation	TaN	ALD TiN, WCN,TaN SiC list cap	Electro grafting Electroless Cu/ Self aligned barrier	4 points bending
Planarization	ECMD cu			
Slurries expertise center		Slurries optimization		
Etch, Strip, CMP, Clean		Reducing strip chemistries, Dry strip wet, clean, Super critical cleaning		Mechanical and adhesion characterization

3D integration

Wafer to wafer direct bonding







CMOS to CMOS capacitive coupling for high speed communication

Direct bonding with capa pad alignement

European High TREE project

Die to wafer direct bonding

Photonic interconnect layer on CMOS

InP dies (1x1 mm^2, alignment accuracy 50 µm)

European PICMOS project

Nanotec 300 running devices projects

- SON based CMOS
- Strained channels
- SG FD SOI
- FinFET-TriGate
- DG MOS
- GeOI MOS

- PD SOI *
- e DRAM *

* projects developed at Crolles

Ebeam R : 25 – 10nm

High K / Metal gate

Strained layers

Selective epi

SiGe isotropic etch

NiSi, NiSiGe, NiGe

CMP, clean

Surface chemical engineering

SOI

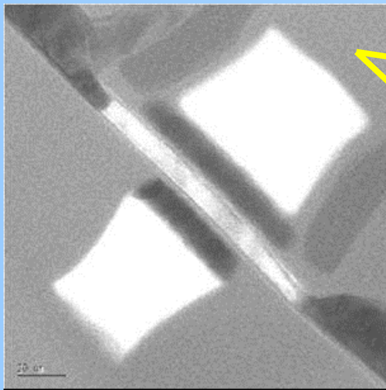
New substrates

Bonding techniques

TEM, ATR, MIR, MEIS

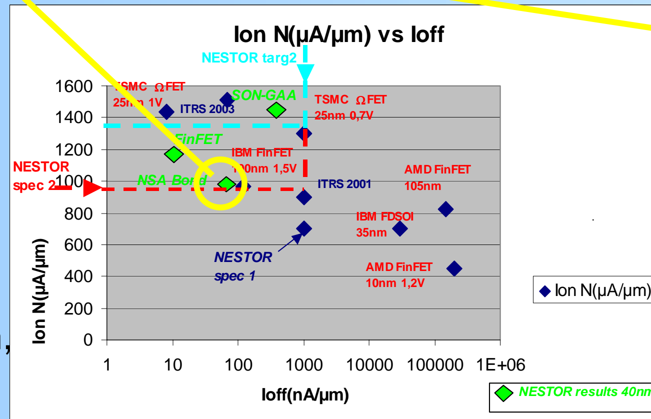
AFM3D, EP

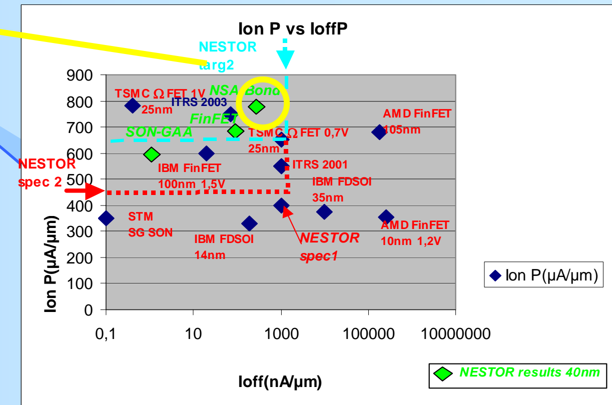
Devices - highlights



Double gate transistor

obtained at **CEA-LETI** using a wafer-bonding technology



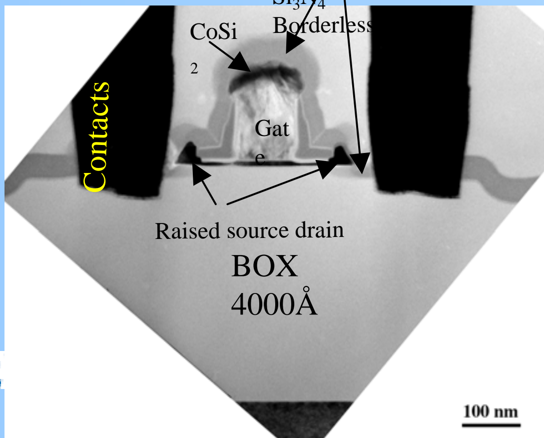


channel Si thickness 10nm,

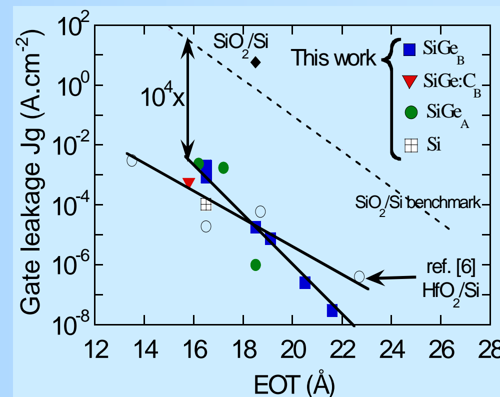
drawn gate length 50nm

FDSOI

SEG on ultrathin Soi films



Heterostructure devices



Short channel effect reduction by using **SiGeC** layers as a **dopant diffusion stopper and compatibility with the high k/metal gate stack**

Focus, aggressive projects

- Focus

  on SOI : ~~Optimization on Bulk~~

  on high K , metal gate

- Focus and aggressive projects

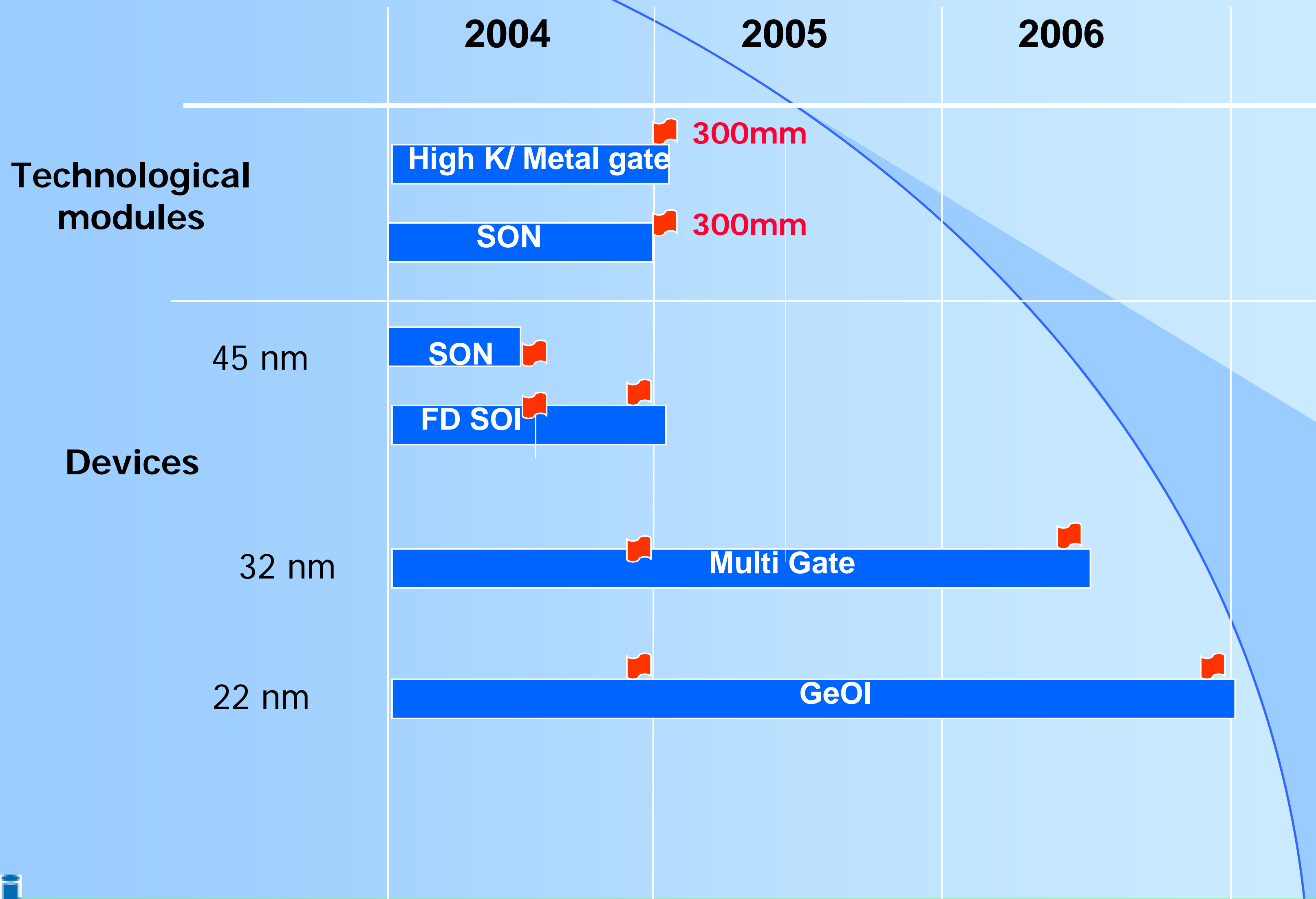
  High mobility

  - FD SOI & Strained channels
  - FD GeOI

  Scaling

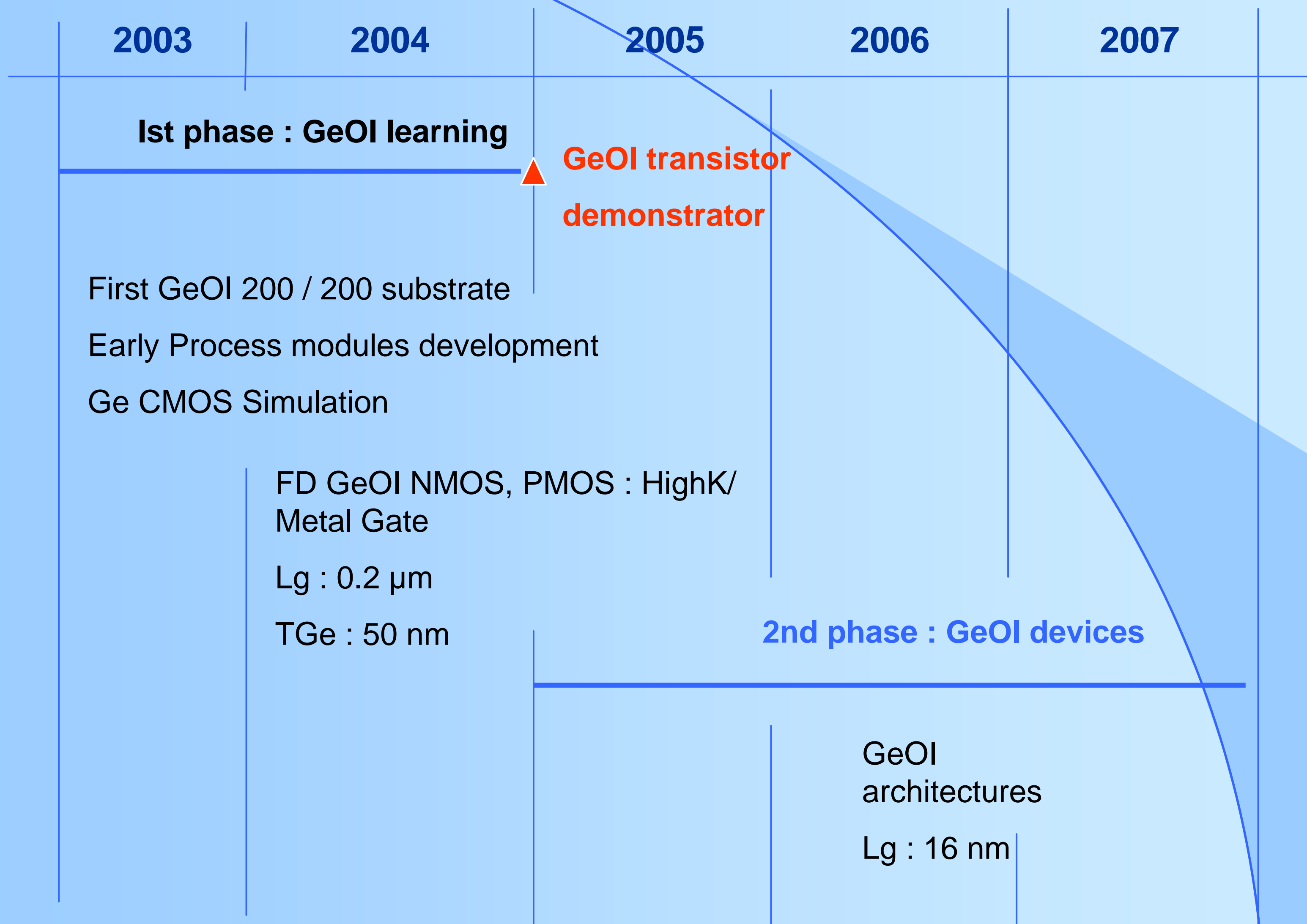
  - Trigate – Fin FET : learning – promising approach
  - Double gate by bonding : original approach
  - Modeling / simulation

6 Flag demonstrators launched in 2004



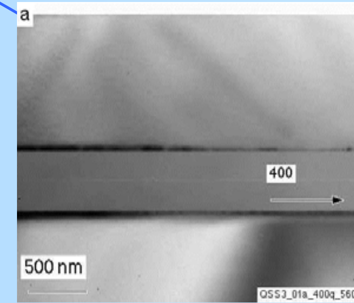
GeOI program

Open Basic Technologic Research



FD GeOI project – recent results

First 200mm Smart-cut ™ GeOI

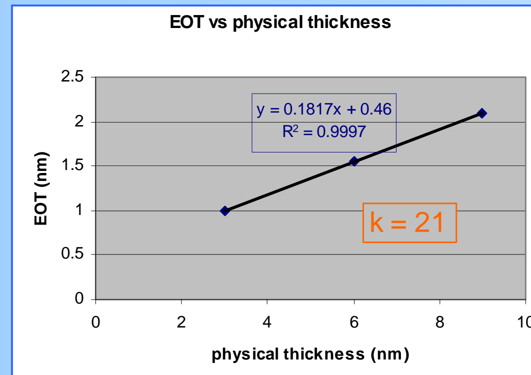


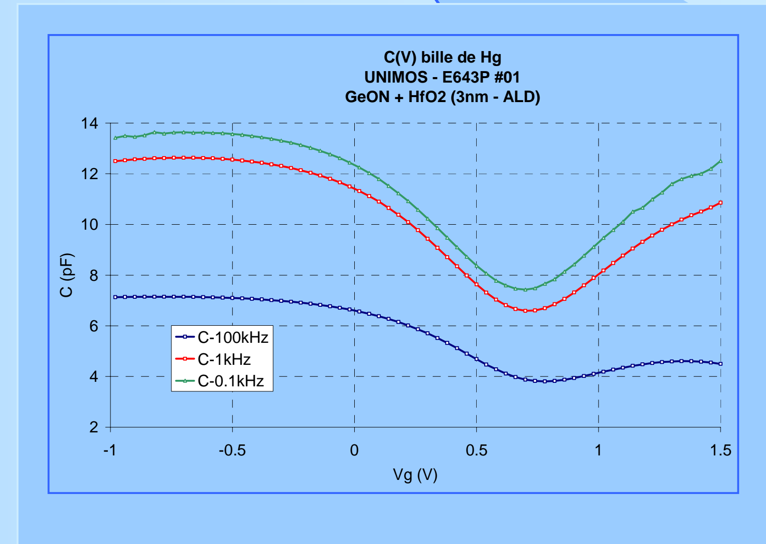
Leti Ge epi

Rms : 0.2 nm

Dislocation <10^6 cm^{-2}

EOT = 1nm (HfO2 = 3 nm)





Leti positioning in Si based memory

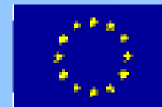
- ✓ In collaboration with the Alliance : SRAM, eDRAM

- ✓ Many collaborations on NVM

  Si Nanocrystals floating gate NVM

  - Scaling : Optimization of process step at the bit cell level
    - Crested barrier, highk, Si dots…
  - New architecture development at the bit cell level
    - FinFlash
  - Design – Technology coupling for validation on array

NANOTEC 300 open to EUROPE



Research institutes

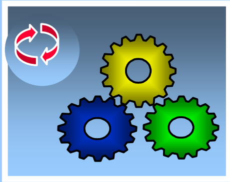
NMRC
FhG
CSEM
IMEC

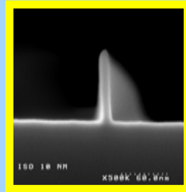
Equipment / material suppliers

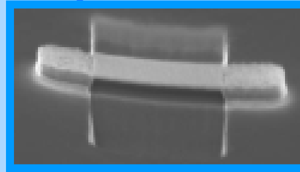
AIXTRON
IBS
Ion TOF
FEI
RECIF
AMAT
AIR LIQUIDE
CARL ZEISS
ASM-E
RUDOLPH
INORTECH
SOPRA
SOITEC
TRIKON
TRACIT
ALCATEL/ADIXEN
ROHM & HAAS
SEMITOOL
HORIBA / JOBIN-YVON
SEZ
ISILTEC
XENOCS
SAGEM
ELDIM

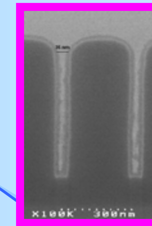
Semiconductor manufacturers

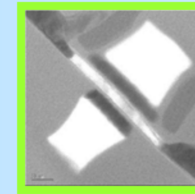
ST
PHILIPS
FREESCALE
ATMEL
INFINEON
ALTIS
AMD











Nanotec 300 program centered on core CMOS technology, structured by an interactive model of plateforme based on short loops with industrial partners, working in competence centers driven by specific roadmaps and a coherent project strategy……………………………….

Thank you for your attention

Extra slides

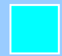
Characterization expertise

X Ray

XRD, XRR, XRF , ESRF : GISAXS (ULK porosity, HiK), µDRX (stress in Cu line)

Optical Analysis

Ellipsometry DUV-IR (ULK), IR spectrophotometry : MIR, ATR, Raman spectrometry – UV Raman (strain)



Surface & Ion Beam

XPS, AES, RBS , MEIS (all elements, diffusion @ interfaces, strain, thin layers)

Microscopy

HR TEM, EELS, STEM, TEMH

Near Field Microscopy

SSRM, SCM (2D profiling), KFM (metal Wf), I(V)4 probes (ultra thin layers)

Ion Beam Analysis

SIMS (1D dopant profile), TOF SIMS (localization, insulator, wide range of elements)

Metrology in line & ultra clean

AFM 3D, XRR, TXRF, VPD – LPD ICPMS , WDXRF, MEB, thickness, …

Lithography related projects

National projects
IST projects
MEDEA projects

2003 | 2004 | 2005 | 2006 | 2007

MEDEA Excite — EUV experimental bench (BEL), outgassing, scatterometry

MEDEA Extumask — Mask Blank and nanopatterning of EUV reflective mask

MEDEA EUVSource — CEA-DSM : LPP Source

IST MoreMoore — EUV Resist, Blank Mask, Phase Shift mask

MEDEA Maskless — E beam

IST Napa — Nanopatterning : Ebeam patterned mold

IST / NMP x beam

MEDEA Liquid

MEDEA Emback

MEDEA MUSCLE

NMP/IST resist, maskless

Back End related projects

National projects
IST projects
MEDEA projects

	2003	2004	2005	2006	2007

IST Ulisse — 65nm – ULK integration k : 2.2

MEDEA T207 — 65nm - ULK integration SRAM

IST NanoCMOS — Nanoporous dielectric integration for 45nm and 32 nm, Air gap, Copper reliability

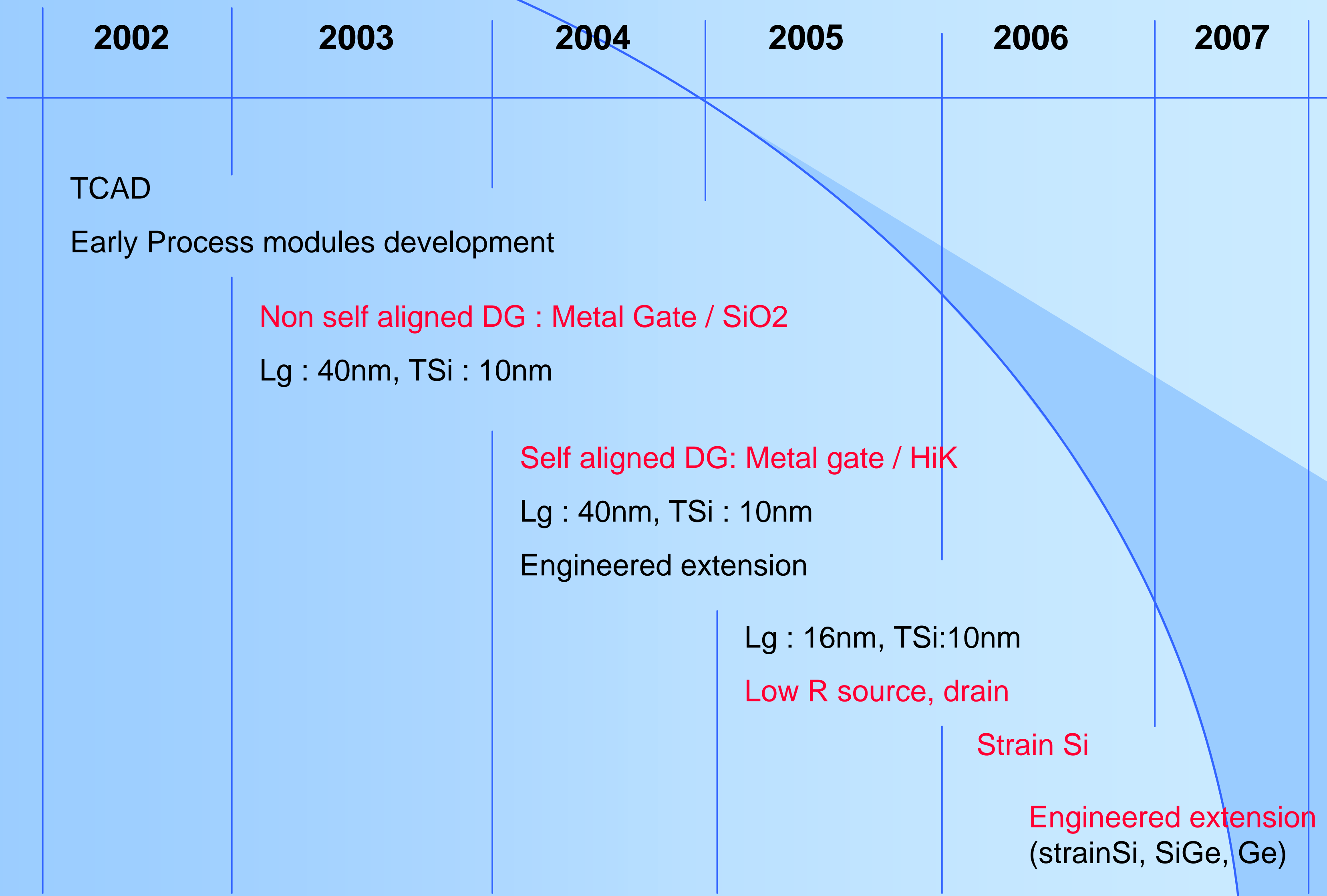
MEDEA HYMNE

MEDEA 45nm

IST / NMP

Fin FET program

Bonded Planar Double Gate program



Planar Double Gate related projects

- National projects
- IST projects
- MEDEA projects

Project	2003	2004	2005	2006	2007
IST V PCRD Nestor	Non Self-Aligned Double gate CMOS				
RMNT CMOSDALI	Self Aligned Double Gate CMOS				
IST NanoCMOS		Improved Self Aligned Double Gate for 45nm – 32 nm			
MEDEA 45nm					
NE Sinano		Network of excellence related to new architectures, new materials			
IST NMP / IST					

Si Nanocrystal memory

	65nm	45nm	32nm	22nm
Nanocrystals floating gate memory	■■■■	▨▨▨▨ (Barrier height modification (high K) – metal dots – self assembly)		
Fin Flash (embedded)		■■■■	■■	
Other concept			■■■■	■■■■
Basic research	■■■■	■■■■	■■■■	■■■■

Basic research
- *Materials*
  - *nano dots, dielectric*
- *Architecture*
- *Single dot physics*

National projects
IST projects
MEDEA projects

Si Non Volatile Memory related projects

	2003	2004	2005	2006	2007

Région SiNanocrystals — Si nanocrystals deposition , characterization, properties

Région DotSET — Localization of a single Si Nc - SET

V PCRD Adamant — Demonstration of NVM 1 Mb with trapped floating gate (SiNc, SiN..)

MEDEA NEMeSyS

NMP UV LS MO CVD

IST/NMP FinFlash

RMNT materials

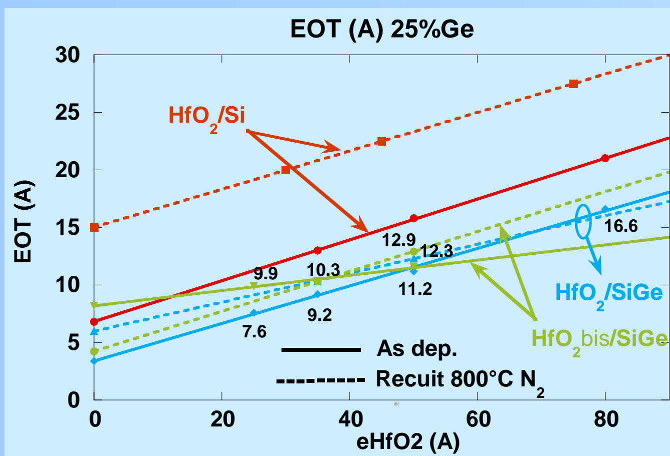
Leti

Front End Materials & Processing highlights

High k dielectrics

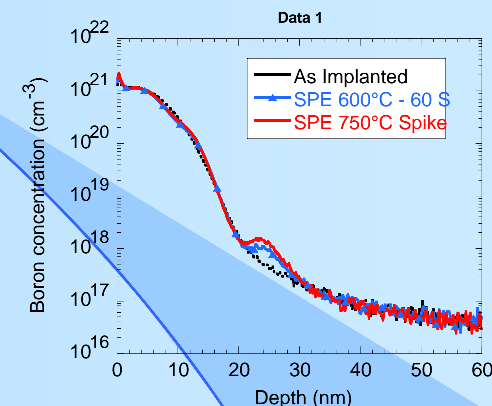
In depth analysis of the nitridation of HfSiO films

Very low EOT HfO2 / SiGe compared to Si



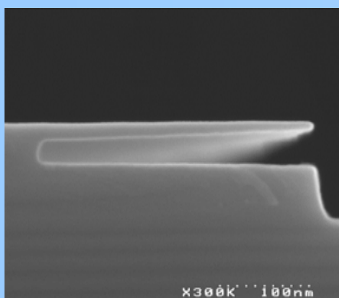
USJ

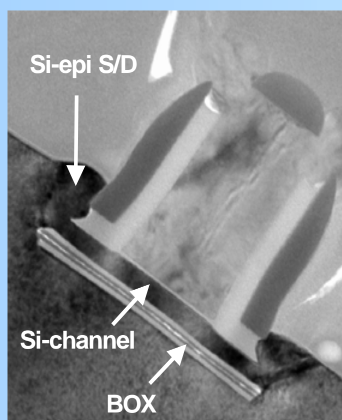
Very low dopant diffusion after SPE



Epitaxy

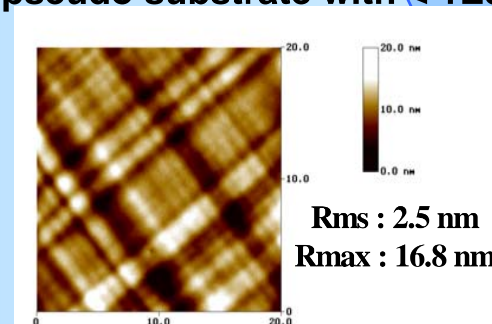
SiGe selective etch for SON





SON device (ST/LETI)

SiGe pseudo substrate with < 1E5 def/cm²



AFM image of the surface of a SiGe 20% virtual substrate grown at 850°C

Front End related projects

National projects
IST projects
MEDEA projects

	2003	2004	2005	2006	2007
Gate stack					
RMNT Kappa	HfO2 dielectric – poly gate				
Region OXEPISI	Alternative HfO2 dielectric (LaAlO3-MBE)				
NMP /IST					
Source, Drain					
RMNT Dolami	10nm deep junction – Laser activation / laser doping				
IST/ NMP					
MEDEA T303	Activation of dopant - Levitor				
Integration					
MEDEA T207	65nm HK/SiON – poly gate				
IST NanoCMOS	45nm HK/Metal gate, Raised S/D,				
MEDEA 45nm					