

EE597: RF MOSFET MODELING (SPRING 2005)
SUGGESTED READING LIST

Models & Parameter extraction:

1. M. Hu, et .al, "An analytical Fully depeleted SOI MOSFET model considering the effects of self heating, source drain resistance, impact ionization, and parasitic BJT," Japanese J. Appl. Phys., Vol. 36, pp. 2606-2613 (1997).
2. J.A. Power, " An enhanced SPICE model suitable for analog applications," IEEE Trans. Computer-Aided Design, vol. 11, pp. 1418-1425, 1992.
3. Y. Tsvividis and G. Masetti, "Problems in Precision Modeling of the MOS Transistor for analog applications," IEEE Trans. Computer-Aided Design, vol. 3, pp. 72-79, 1984.
4. A. Silburt, "An efficient MOS transistor Model for Computer-Aided design," IEEE Trans. Computer-Aided Design, vol. 3, pp. 104-111, 1984.
5. M.F. Hammer, "First-order parameter extraction on enhancement silicon MOS Transistors," IEE Proc. Vol. 133, Pt. 1, pp. 49-56, 1986.
6. R. Troutman, "VLSI limitations from Drain-Induced Barrier Lowering," IEEE Journal of Solid State Circuits, Vol. 14, pp. 383-390, 1979. (good discussion of DIBL).
7. G. Merckel, "A simple model of the Threshold voltage of Short and Narrow Channle MOSFETs," Solid State Electronics, Vol. 23, pp. 1207-1213, 1980.
8. G.W. Taylor, "Subthreshold Conduction in MOSFET's," IEEE Trans. Electron Devices, Vol. 25, pp. 337-350. (good discussion).
9. L.A. Akers and J.J. Sanchez, "Threshold Voltage Models of Short, Narrow, and Small geometry MOSFET's,: a Review," Solid State Electronics, Vol. 25, pp. 621-641, 1982
10. M.A. Imam, H. Fu, M.A. Osman, and A.A. Osman, "A Simple Method to Determine the Floating-Body voltage of SOI CMOS Devices," IEEE Electron Device letters, Vol. 21, pp. 21-23, 2000.

RF Modeling:

1. S. M. Jen, C.C. Enz, et..al "Accurate Modeling and Parameter Extraction for MOS Transistors valid up to 10GHz", IEEE Trans. Electron Devices, Vol. 46, pp. 2217-2226, 1999. (see also references 4,5,6,7,10,11, and 14).
2. E. Abou-Allam and T. Manku, "A small signal MOSFET model for Radio Frequency IC Applications," IEEE Trans. Computer-Aided Design, vol. 16, pp. 437-447, 1997. (see also references: 2 and 4).

NOISE:

1. G.O. Workman and J.G. Fossum, "Physical Noise Modeling of SOI MOSFET's with Analysis of the Lorentzian Component in the Low-Frequency Noise Spectrum," IEEE Trans. Electron devices, Vol. 47, pp. 1192-1200, 2000. (see ref. 2-9 for noise in SOI).
2. W. Jin, P.C.H. Chan, and J. Lau, "A physical Thermal Noise Model for SOI MOSFET," IEEE Trans. Electron devices, Vol. 47, pp. 768-772, 2000
3. J.H. Scofield, et. al, "Reconciliation of different gate-voltage dependencies of 1/f noise in n-MOS and p-MOS Transistors," IEEE Trans. Electron devices, vol. 41, pp. 1946-1952, 1994.
4. R.P. Jindal, "Noise associated with Substrate Current in fine line NMOS FETs," IEEE Trans. Electron devices, vol. 32, pp. 1047-1052, 1985.
5. P.L. Olsen, "Evaluate 1/f effects on oscillator phase noise," Microwaves and RF, pp. 82-93, August 1997.
6. B. Glodberg, "Phase Noise Theory and Measurements: A short review," Microwave Journal, pp. 112-122, January 2000.

Device Simulation:

On-line ISE TCAD manual and examples.

S-parameters and RF measurements:

1. S.J. Parsad, "Take the Fog Out of S-parameters," Tektronix Technical report # SSRL-89-1.
2. "ON Wafer Vector Network Analyzer Calibration and Measurements," Cascade Microtech Application note.

Nanoscale MOSFETs (FINFETs, etc) : (links will be provided for the following papers)

1. B. Doyle, R. Arghavani, et.al, "Transistor Elements for 30 nm Physical Gate Lengths and Beyond," Intel Technology Journal, Vol. 6, May 2002.

http://www.intel.com/technology/itj/2002/volume06issue02/art05_transistorarch/p01_abstract.htm

2. B. Yu, L. Chang, S. Ahmed, .."FinFET scaling to 10 nm Gate Length," 2002. (AMD group)