

1. Derive the expressions for the depletion width in a linearly graded p-n junction.
2. The measured values of the junction capacitance are given in figures 1 and 2 (to be handed in class) for two sets of areas and perimeters. From each curve set up a $C(V)$ table (e.g at 0.25 to 0.5 v step) and setup tables for C_{JA} and C_{JP} . Extract the values of C_j , M_j , PB , C_{jsw} , M_{jsw} , PB_{sw} . Plot C_{JA} and C_{JP} . Assume 0.847 V built in potential.
3. An ideal silicon MOS Capacitor with 500Å gate dielectric (SiO_2) formed on a substrate doped to $N_A=3 \times 10^{15} \text{ cm}^{-3}$. Assuming $T=300 \text{ K}$. Determine the following:
 - a. Insulator capacitance C_i
 - b. Minimum capacitance C_{\min} using depletion approximation,
 - c. Threshold voltage V_T
 - d. Plot the $C(V_G)$ characteristics for this capacitor.
 - e. Sketch another $C(V_G)$ on the same plot if the substrate doping is increased. Indicate all the qualitative changes due N_A increase.
4. An ideal silicon MOS Capacitor with 50Å gate dielectric (SiO_2) formed on a substrate doped to $N_A=10^{16} \text{ cm}^{-3}$. Assuming $T=300 \text{ K}$. Determine the following:
 - a. Capacitor area required to give $C_i = 10 \text{ pF}$
 - b. Values of V_T , C_{\min} , and C_{FB}
 - c. Sketch the high frequency $C(V_G)$ curve.
5. A MOSFET process uses a gate dielectric of 250 Å thickness with p-type substrate doped to 10^{16} cm^{-3} . The gate material is n+ polysilicon (assume that $\Phi_m = \Phi_{(\text{poly})} = 4.05 \text{ eV}$) and the MOS is otherwise ideal.
 - a. Write a program (matlab or any other language) to predict the threshold voltage over the commercial temperature range (-25C to 85C). Plot the results.
 - b. Determine the temperature coefficient [mV/C] at 25 C. Can the temperature dependence be modeled by a constant temperature coefficient over this range [-25 to 85 C] ?
 - c. Mm