A Unified Error Control Coding Scheme to Enhance the Reliability of a Hybrid Wireless Network-on-Chip

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Abstract—Hybrid wireless Network-on-Chip (NoC) has emerged as an alternative to the traditional multi-hop wireline NoC to achieve higher performance and low energy dissipation in on-chip data transfer. However, introduction of on-chip wireless links lowers the overall reliability of the data communication fabric. In this paper we propose a unified Error Control Coding (ECC) mechanism which can be effectively used to restore the reliability of a Wireless NoC (WiNoC). We demonstrate that with carefully designed ECC schemes in the WiNoC it is possible to achieve high gains in performance due to the wireless links while maintaining comparable reliability as that of a traditional wireline NoC.

Keywords—Network-on-Chip, Error Control Coding, Wireless Interconnects

I. INTRODUCTION

Design of multi-core integrated systems beyond the current CMOS era will present unprecedented advantages and challenges, the former being related to very high device densities and the latter to soaring power dissipation issues. According to the International Technology Roadmap for Semiconductors (ITRS) in 2007, the contribution of interconnects to chip power dissipation is expected to increase from 51% in the 0.13um technology generation to up to 80% in the next five year period. This clearly indicates the future design challenges associated with traditional scaling of conventional metal interconnects and material innovation. To enhance the performance of conventional metal interconnect-based multi-core chips, a few radically different interconnect technologies are being currently explored such as 3D integration [1], photonic interconnects [2] and multi-band RF [3] or wireless interconnects [4]. All these new technologies have been predicted to be capable of enabling multi-core designs, which improve the speed and power dissipation in data transfer significantly. However, these alternative interconnect paradigms are in their formative stages and need to overcome significant challenges pertaining to reliability. Error Control Coding (ECC) has emerged as a viable solution to increase the reliability of on-chip communication links [5]. It has already been demonstrated that specially designed ECCs increase reliability as well as lower energy dissipation of traditional NoC links [6]. In this paper we address reliability issues in a hybrid wireless NoC (WiNoC) [7] by proposing a unified ECC framework with different schemes for wireline and wireless links. Wireless links in the hybrid NoC encounter higher error rates than regular wires and hence stronger ECC schemes are required to restore the reliability on such links. In this work we determine the typical error rates of the on-chip wireless links and propose suitable ECC mechanisms to improve their reliability. We demonstrate that using the proposed unified ECC scheme it is possible to achieve significantly low energy dissipation and high bandwidth in a wireless NoC while still maintaining similar reliability to that of a regular wireline counterpart.

II. RELATED WORK

ECC schemes have been explored in the context of NoC links to enhance the reliability of data transmission and reduce energy dissipation. In the Ultra-Deep Submicron (UDSM) technologies crosstalk coupling between adjacent wires as well as several transient error mechanisms like ground bounce and alpha particles result in increased probability of multi-bit errors. In
In generic wired NoCs the constituent embedded cores communicate via multiple switches/routers and wired links. This multi-hop communication results in data transfers with high energy dissipation and latency. One of the promising ways to alleviate this problem is to establish long-range, low-power and high bandwidth wireless links between distant parts of the chip. Carbon Nanotube (CNT) based antennas have been recently demonstrated to perform similar to radio antennas and exhibit directional radiation characteristics [14]. By using such CNT antennas on-chip wireless links operating in the range of THz frequencies can be established. Besides providing true-speed-of-light data exchange between source and destination pairs such wireless links also dissipate orders of magnitude less power than traditional wireline links of the same length [7]. Due to these advantages a NoC designed with long-range wireless links can outperform its traditional wireline counterparts to deliver extremely high network bandwidth while considerably reducing the energy budget. As the wireless channels can be used to establish long distance links, they can be introduced as shortcuts within an existing NoC to enhance connectivity. Following this basic principle, the design philosophies of a wireless NoC (WiNoC) were elaborated in [7]. The proposed design was a hierarchical, hybrid wired/wireless NoC architecture. The whole NoC is divided into smaller clusters called subnets. The subnets form the lower level of the hierarchy. Cores within a single subnet communicate via traditional wired links connected in regular topologies, e.g., mesh, star or tree as shown in fig. 1. Each subnet is equipped with a hub where the cores are connected to the hubs with direct links. The hubs are connected following the principles of small-world networks [15] in the 2nd level of hierarchy. A small-world topology can be constructed from a locally connected network by re-wiring connections randomly to any other node, which creates short cuts in the network. Such a trade-off between a completely regular network and a completely random network has the distinct advantage of having both a very short average number of hops between the nodes as well as a high degree of connectivity. Thus the hubs are connected in a small-world network with wireline links between neighboring hubs and a few wireless shortcuts between distant hubs as shown in fig. 1. Instead of the ring shown in the figure the hubs may also be connected using other topologies such as mesh.

The number and placement of the wireless links between the hubs depend on the number of distinct frequency channels that can be created using the CNT antennas. The placement of the wireless links can be optimized to obtain the best performance in terms of chosen metrics like network throughput, latency or energy dissipation. In order to optimize the network configuration with respect to the placement of the wireless links various optimization approaches can be undertaken, vis-à-vis simulated annealing (SA), gradient descent or even an exhaustive search. However with increase in system size exhaustive search can be prohibitively time-consuming as the size of the search space grows at a combinatorial rate. Discounting adjacent hubs as they are already connected by the normal wired links the size of the search space is given by

$$|S| = \binom{N}{n}$$

where $N$ is the number of hubs in the network and $n$ is the number of wireless links to distribute. The metric for optimization must be properly designed to represent the important performance metrics of the WiNoC. The approach adopted was to insert the long range links between distant nodes which also communicate frequently. Hence, the optimization metric was the average distance between all source and destination pairs weighted with the probability of communication between them. The chosen metric, $\mu$ is given by

$$\mu = \sum_{i,j} h_{ij} f_{ij}$$

where $h_{ij}$ is the minimum distance in number of hops between source node $i$ and destination node $j$, and $f_{ij}$ is the probability of communication between source $i$ and destination $j$. This metric incorporates the effects of non-uniform traffic patterns in the NoC and optimizes the network topology by placing the wireless links between frequently communicating distant hubs that
would otherwise negatively affect the NoC performance if the long-range wireless shortcuts were not inserted. We adopted the SA heuristic to determine the optimal distribution of the wireless links due to its scalability with increase in system size.

Within the subnets, data packets are routed using wireline links. When packets need to travel across subnets then the shortest path in terms of number of hops is chosen in the small-world network which has both wireline and wireless links. By using multiband laser sources to excite CNT antennas, different frequency channels can be assigned to pairs of communicating subnets. This will require using antenna elements tuned to different frequencies for each pair, thus creating a form of frequency division multiplexing (FDM) with dedicated channels between a source and destination pair. This is possible by using CNTs of different lengths, which are multiples of the wavelengths of the respective carrier frequencies. The high directional gains of these antennas [14] aid in creating directed channels between source and destination pairs. In [16], 24 continuous wave laser sources of different frequencies are used. Thus, these 24 different frequencies can be assigned to multiple wireless links in the WiNoC in such a way that a single frequency channel is used only once to avoid signal interference on the same frequencies. This enables concurrent use of multi-band channels over the chip. The number of wireless links in the network can therefore vary from 24 links, each with a single frequency channel, to a single link with all 24 channels. It is shown in [7] that having all the available channels allocated to different links maximizes the performance of the WiNoC as it increases the connectivity of the network for the available total wireless bandwidth. Hence, in this work we distribute all the available channels into different links with each link having a single frequency channel. In each channel it is possible to maintain a data rate of 10Gbps [17] using high speed silicon integrated Mach-Zehnder modulators and demodulators. The modulation scheme adopted is non-coherent on-off keying (OOK), and therefore does not require complex carrier recovery and synchronization circuits.

B. Reliability in WiNoCs

Aggressive scaling in the nanometer technology nodes result in inherently unreliable or defect prone devices. The performance of the wireless links in the WiNoC depends on the CNT antennas. Like any other nanodevices, CNT antennas are expected to have higher manufacturing defect rates, operational uncertainties and process variability [18].

Error Control Coding (ECC) has been proposed for mitigating the inherent reliability issues in on-chip communication [5]. Defect-prone CNTs can lead to relatively high random error rates and cause multi-bit errors or burst errors. Therefore the coding scheme should be robust against both random and burst errors. As a first step, in the next subsection we present a model of the on-chip wireless channel and evaluate the corresponding bit error rates. In latter subsections we propose and evaluate ECC schemes for the on-chip wireless links and for the wired links, in order to improve the reliability of a WiNoC.

1) Wireless Channel Model

By elevating the chip packaging material from the substrate to create a vacuum for transmission of the high frequency EM waves, LOS communication between WBs using CNT antennas at optical frequencies can be achieved. Techniques for creating such vacuum packaging are already utilized for MEMS applications [19], and can be adopted to make creation of LOS communication between CNT antennas viable. However, reflection from the surfaces of the substrates and the packaging material interfere with the LOS transmitted power. In the channel model we account for the multipath reflection from all 6 surfaces of the packaging as well as the thermal noise coupled to the received signal from the LOS transmission. Fig. 2 shows the multipath transmission of the signal from the transmitter to the receiver with all the possible reflected rays from four walls, ceiling and ground. The total received power is given by

\[
P_r = \frac{A_r}{4\pi} P_t \left( \frac{G_{T,LOS} e^{-j\frac{2\pi}{\lambda} R_{LOS}} + \Gamma_1 G_{T_1} e^{-j\frac{2\pi}{\lambda} R_1} + \Gamma_2 G_{T_2} e^{-j\frac{2\pi}{\lambda} R_2} + \Gamma_3 G_{T_3} e^{-j\frac{2\pi}{\lambda} R_3} + \Gamma_4 G_{T_4} e^{-j\frac{2\pi}{\lambda} R_4}}{R_{LOS}} \right)^2
\]

where \(G_{T,LOS}\) is the transmitter antenna gain along the LOS, which is shown to be -5dB [14]. \(A_r\) is the area of the receiving antenna and \(R_{LOS}\) is the LOS distance between the transmitter and receiver. \(R_1, R_2, R_3, R_4, R_{ceiling}\) and \(R_{ground}\) are the distances along the different reflected paths. \(\Gamma_1, \Gamma_2, \Gamma_3, \Gamma_4, \Gamma_{ceiling}\) and \(\Gamma_{ground}\) are the coefficients of reflections on the substrate and packaging surfaces obtained from [20]. \(G_{T_1}, G_{T_2}, G_{T_3}, G_{T_4}, G_{T,ceiling}\) and \(G_{T,ground}\) are the antenna gains along the directions of the reflected paths which are all less than -10dB [14]. Due to low coefficients of reflection of the packaging materials and high
directional gains of the antennas only primary reflections are considered in this model. Subsequent reflections will diminish the reflected power further and may be neglected in this case. The thermal noise power is given by

\[ N_0 = kT_0F = kT_0 \left( \frac{T_{\text{antenna}}}{T_0} + F_r \right). \] (4)

where \( k \) is the Boltzmann constant, \( T_0 \) is the room temperature taken as 290K, \( T_{\text{antenna}} \) is the antenna temperature assumed to be 330K, and \( F_r \) is the receiver noise figure of 4dB [21]. The coupling of the chip switching noise to the wireless channels is negligible as the wireless channels are in very high frequency bands of a few THz. Hence, the Signal-to-Noise Ratio (SNR) is given by

\[ \text{SNR} = \frac{P_R}{N_0}. \] (5)

Fig. 3 shows the variation of the SNR over the 20mm x 20mm die area for a fixed position of the transmitter. The transmitter in this case is placed at the center of the subnet at the near corner in fig. 3. The received SNR is the maximum near the transmitter and gradually diminishes with distance. Even though there is multipath reflection from the substrate and packaging walls, the reflected power is negligible as signified by the quadratic variation of the received SNR with distance in fig. 3. This is due to low coefficient of reflection of the reflecting surfaces and high directivity of the antennas which attenuate the radiations in the directions other than the LOS. The SNR vs. bit-error-rate (BER) characteristics for the wireless links correspond to the adopted modulation scheme, which is non-coherent OOK. Fig. 4 shows the variation of BER with SNR for a non-coherent OOK receiver. The particular configuration of the wireless links established for optimal network performance by simulated annealing places the 24 links between specific subnets in the WiNoC. The SNR and hence the BER corresponding to those links are also marked with circles in the plot. The SNR and hence the BER on those 24 links varies as each link is of a different length resulting in different path loss and reflected radiation patterns. However, some of the 24 links have the same SNR and hence appear as the same point on the plot. As can be seen the highest BER for the wireless links on the chip is around 4\( \times 10^{-4} \). Since this is the highest BER among all the wireless links it can be referred to as the effective BER of the WiNoC. This effective BER of the WiNoC is much higher than the BER of wireline links, which is typically around \( 10^{-15} \) or less [5]. Hence, we propose using powerful multiple/burst error correction codes for the wireless channels. In the next subsection we describe a product code based ECC to enhance the reliability of the wireless links.

2) Proposed Product Code for the Wireless Links

In order to achieve simultaneous random and burst-error correction on the wireless links simple Hamming code based product codes (H-PC) are proposed in this work. The authors of [13] have already shown that product codes designed from simple single error correcting Hamming codes in 2 dimensions can perform better than multiple error correction codes like Bose-Chaudhuri-Hocquenghem (BCH) codes or Reed-Solomon (RS) codes in terms of trade-offs between overall performance and overhead. In this work we propose to use a simple product code which achieves multiple error correction as well as burst error correction of data transmitted through the wireless links. Fig. 5 schematically shows the product code structure. Let us assume a flit size of \( k_1 \) bits and a block of \( k_2 \) such flits. \((n_1, k_1)\) Hamming encoding is performed in the spatial dimension on the flits. Each of the \((n_1, k_1)\) Hamming encoded flits are then encoded using \((n_2, k_2)\) Hamming encoding is done in the time dimension to give a \((n_1 \times n_2, k_1 \times k_2)\) product code.

![Figure 3. SNR over the die area due to multipath radiation from a transmitter placed in the first subnet at its center (X=2.5mm, Y=2.5mm).](image3)

![Figure 4. SNR vs. BER plot of the wireless channel with and without coding.](image4)
code. In our work, we chose a (38, 32) shortened Hamming code in the spatial dimension to encode a whole 32 bit flit at a time. In the time dimension a (7, 4) Hamming code is chosen to minimize the latency and buffering overheads of storing a block of bigger size. Any bigger code would cause higher buffering requirements at the wireless nodes in the WiNoC. The product code decoder utilizes a row-column decoding technique where first the (38, 32) Hamming decoder operates on the received columns of the block and then the (7, 4) Hamming decoders decode the rows to give back the 4 received 32 bit flits. This decoding technique is referred to as column-first decoding. In order to mask the latency penalty of the decoding, the decoder is designed such that the (38, 32) Hamming decoder operates on the received flits as they arrive and parallel (7, 4) Hamming decoders then operate in parallel on the received 32 bit flits. This minimizes the latency overhead of the H-PC decoder.

3) Residual BER of the Wireless Channel with H-PC

In order to estimate the effectiveness of the proposed coding scheme we perform a residual BER analysis after implementing the ECC. This analysis is based on the smallest weight error events that are uncorrectable by the product code, since these events will dominate the BER at high SNR. Fig. 6 shows the various correctable and uncorrectable error patterns in a block of size \( n_1 \times n_2 \) for the row-column decoding technique. The scenario shown in fig. 6(a) has a spatial burst along a particular flit represented by the shaded column, as well as single bit random errors in other flits. This can be corrected if column decoding is done first followed by row decoding, as in the adopted column-first decoding. The column decoding will correct all the random errors but not the burst, which, however, will be corrected by row decoding. For the scenario in fig. 6(b) with a single burst in time and some random errors, the column-first decoding scheme will correct all errors if the uncorrectable error patterns on the columns produce correctable error patterns on the rows after column decoding. However this case is not likely to occur because each antenna is responsible for transmission of multiple bits in the same flit before transmitting bits of another flit. The case shown in fig. 6(c) with a burst in each direction can be corrected completely, as column decoding will correct the burst in time except the top left bit. The resulting pattern is only a burst in space which can be corrected by row decoding. Rectangular error patterns as shown in fig. 6(d), cannot be corrected by row-column decoding because double errors occur in both rows and columns. This is the highest probability event as only 4 erroneous bits in a whole block lead to uncorrectable error patterns. The probability of this event is given by

\[
P_{\text{rectangle}} = N_{\text{rectangle}} \varepsilon^4 (1 - \varepsilon)^{n_1 n_2 - 4}
\]  

(6)

where \( N_{\text{rectangle}} \) is the number of rectangular patterns possible in a block of size \( n_1 \times n_2 \) and \( \varepsilon \) is the BER without coding. \( N_{\text{rectangle}} \) is computed as

\[
N_{\text{rectangle}} = \sum_{l=2}^{n_1} \sum_{b=2}^{n_2} (n_1 - l + 1)(n_2 - b + 1)
\]  

(7)

At high SNR where the highest probability events dominate the BER, the residual BER with the product code is given by

\[
\varepsilon_{\text{PC}} = \left( \frac{1}{n_1 n_2} \right) P_{\text{rectangle}}
\]  

(8)

The new SNR vs. residual BER on the particular wireless links are shown in fig. 4 after implementing the product code with squares on a dotted line. The effect of the product code is to significantly lower residual BER. The worst case BER on the link with the lowest SNR is 1.99x10^{-12}. This reduction in BER gives a higher level of reliability compared to the uncoded system. In addition, the worst case BER of the wireless channel becomes comparable with the BER in the wireline links by using the H-PC scheme.

4) Error Control Coding for the Wireline Links

In the subnets, the data transmission takes place through the wireline links. It is well known that with shrinking geometry, wireline links will be increasingly exposed to different sources of transient noise affecting signal integrity and system reliability. Data-dependent crosstalk between adjacent wires is also a major source of such transient noise. Due to shrinking feature size in future technologies the transient error rate is predicted to increase by several orders of magnitude. As these errors are not necessarily correlated, higher rate of failures can cause uncorrelated multiple bit errors in data blocks. In [6] a family of joint crosstalk avoidance and multiple error correction codes have been proposed. These codes avoid worst-case crosstalk between adjacent wires as well as correct up to three random errors in a flit and can detect four errors. The underlying idea behind this coding scheme is that the Hamming distance between two Single Error Correcting and Double Error Detecting (SEC-DED) Hsiao code [22] words is 4. Duplication of these encoded bits result in doubling the minimum Hamming distance.
between the code words to 8. Thus it is possible to correct 3 errors in the code word and simultaneously detect any 4-error events. Duplicating the bits and interleaving them beside the original bit lines also serves the purpose of avoiding worst case crosstalk by eliminating opposite transitions on either side of any particular wire. This coding scheme is referred to as Joint Crosstalk Avoidance Triple Error Correction and Simultaneous Quadruple Error Detection Code (JTEC-SQED) [6].

a) Residual BER with JTEC-SQED

To compute the residual word error probability for the JTEC-SQED scheme let us assume that the total number of bits in the flit is $2n+2$, where there are 2 copies of a $(n+1, k)$ SEC-DED codeword. Since JTEC-SQED can either correct or detect up to four errors, the lower bound on the probability of correct decoding can be obtained as

$$P_{\text{correct}} = P(2n+2,0) + \ldots + P(2n+2,4),$$

where $P(i,j)$ is the probability of $j$ random errors in $i$ bits given by

$$P(i,j) = \binom{i}{j} \epsilon^j (1-\epsilon)^{i-j}.$$  

The set of correctly decoded words is complementary to the set of residual word errors. Hence the residual word error probability can be computed using

$$P_{\text{JTEC-SQED}} = 1 - P_{\text{correct}},$$

where $P_{\text{JTEC-SQED}}$ is the residual word error probability in presence of coding and $P_{\text{correct}}$ is the probability of correct decoding. Using (9) and (11) the residual word error probability of the JTEC-SQED scheme for small values of $\epsilon$ can be approximated as:

$$P_{\text{JTEC-SQED}} = \left(\frac{2n+2}{5}\right)\epsilon^5.$$  

Incorporation of error control coding enhances the reliability of the communication channel as it becomes robust against transient malfunctions. Increase in reliability by incorporating coding can be translated into a reduction in voltage swing on the interconnect wires as they can tolerate lower noise margins. This results in a savings in energy dissipation as it depends quadratically on the voltage swing. In this section we quantify these gains by modeling the voltage swing reduction as a function of increased error correction capability.

The cumulative effect of all transient UDSM noise sources can be modeled as an additive Gaussian noise voltage $V_N$ with variance $\sigma_N^2$ [5]. Using this model, the BER $\epsilon$ depends on the voltage swing $V_{dd}$ according to

$$\epsilon = Q\left(\frac{V_{dd}}{2\sigma}\right),$$

where the $Q$-function is given by

$$Q(x) = \frac{1}{\sqrt{2\pi}} \int_x^\infty e^{-\frac{y^2}{2}} dy.$$  

The word error probability is a function of the channel BER $\epsilon$. If $P_{\text{UNC}}(\epsilon)$ is the residual probability of word error in the uncoded case and $P_{\text{ECC}}(\epsilon)$ is the residual probability of word error with error control coding, then it is desirable that $P_{\text{ECC}}(\epsilon) \leq P_{\text{UNC}}(\epsilon)$. Using (13), we can reduce the supply voltage in presence of coding to $V_{dd}$, given by [5]

$$V_{dd} = V_{dd} \frac{Q^{-1}(\hat{\epsilon})}{Q^{-1}(\epsilon)}.$$  

In (15), $V_{dd}$ is the nominal supply voltage in the absence of any coding, $V_{dd}$ is the reduced voltage swing with coding and $\epsilon$ is the BER such that

$$P_{\text{ECC}}(\hat{\epsilon}) = P_{\text{UNC}}(\epsilon).$$  

Use of lower voltage swing makes the probability of multi-bit error patterns higher, necessitating the use of multiple error correcting codes in order to maintain the same word error probability as the uncoded case. As the JTEC-SQED scheme can reduce the voltage swing the most and correct the highest number of errors in a single flit it was chosen for the wireline links of the WiNoC.

Figure 6. (a)-(c): Different correctable error patterns. (d) Uncorrectable pattern.
By using JTEC-SQED on the wireline links of the NoC it is possible to maintain the same level of reliability as without any ECC but with lower energy dissipation due to reduced voltage swing and crosstalk capacitance on the wires. For the wireless links as shown in fig. 4 the BER without any ECC is quite high. However, with H-PC it is possible to achieve the BER comparable to that of the wireline NoC without ECC. We investigated the performance of a WiNoC with a unified coding scheme using JTEC-SQED for the wireline links and H-PC on the wireless links to achieve the same BER as a completely wireline NoC without any ECC. In the following section we present the performance and energy dissipation characteristics of a WiNoC with the unified coding scheme and compare it with a wireline NoC.

IV. EXPERIMENTAL RESULTS

In order to characterize the performance of the proposed coding schemes in a WiNoC, we consider a system consisting of 256 cores. Following the design principles for highest throughput in [7] the WiNoC is divided into 16 subnets each with 16 cores, and the 24 wireless links are distributed among the subnets. The size of the upper and lower level of the hierarchical WiNoC are chosen to be the same so as not to make either one larger than the other resulting in that level becoming the bottleneck. The cores within each subnet are connected with wireline links following a mesh topology. We assume a die size of 20mm x 20mm. The switch and hub architectures are adopted from [7].

The network switches, hubs and codecs for the ECCs are synthesized from a RTL level design using 65nm standard cell libraries from CMP (http://cmp.imag.fr), using Synopsys Design Vision and assuming a clock frequency of 2.5 GHz. The energy dissipation on the wires was obtained from CADENCE Spectre. The energy dissipation on the wireless links was obtained from (3). The WiNoC is simulated using a cycle accurate simulator which models the progress of data flits accurately per clock cycle accounting for flits that reach destination as well as those that are dropped. Fig. 7 shows the packet energy dissipation of the WiNoC with and without the proposed unified ECC scheme. Packet energy dissipation is the energy dissipated in transferring one packet from source to destination. For comparison, the packet energy dissipation in a completely wireline mesh NoC with and without ECC is also shown. The ECC used in the wireline links of the subnets is JTEC-SQED as it is the most energy efficient coding scheme [6]. The effective BER on the communication links in the corresponding cases are also shown. For the mesh with JTEC-SQED, the BER is the same as in the mesh without any ECC as the voltage swing was reduced on the links in accordance with (15). For the WiNoCs the BER on the wireless channels is much higher than that of the wireline links and hence this represents the effective BER on the communication links. As shown in [6] the packet energy of the wireline mesh is reduced due to JTEC-SQED, as the voltage swing on the wireline links can be reduced significantly according to (15). In addition, the crosstalk coupling capacitances on the wires are reduced. The energy savings due to these two factors are more than the overheads due to the codecs and redundant links [6]. The overall reliability on the wires is the same in both cases as the reduction in energy dissipation is projected for the same BER on the wires. For the WiNoC without ECC the worst case BER is much higher due to low SNR. But with the powerful H-PC coding on the wireless channels the BER of the wireless channels are reduced to around $10^{-12}$.

Hence, the overall reliability of the WiNoC is improved with the coding schemes. The overheads of the H-PC scheme and the JTEC-SQED are considered and we find that there is an increase in the packet energy due to the codec overheads of the ECCs compared to the WiNoC without any coding. However, at the cost of this slight increase in packet energy we are able to achieve a comparable overall BER on the WiNoC as that of the completely wireline mesh NoC. The packet energy dissipation of the WiNoC with ECC however still remains several orders of

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<th>Coding Scheme</th>
<th>Encoder</th>
<th>Decoder</th>
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<tr>
<td>H-PC</td>
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<td>354</td>
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<tr>
<td>JTEC-SQED</td>
<td>133</td>
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Figure 7. Packet energy dissipation and worst case channel BER for WiNoC and mesh architectures with and without ECC.

Figure 8. Latency characteristics of mesh and WiNoC architectures with and without ECC.
magnitude lower than that of a complete wireline counterpart due to the low-power long range wireless links.

We also estimate the timing characteristics of the WiNoC in comparison to the wireline mesh. The end-to-end message latency of the wireline mesh with JTEC-SQED is higher than that of the mesh without ECC. This is because the ECC codecs add overheads to the critical paths in the NoC switches. The WiNoC without any ECC achieves a much lower latency compared to the wireline network due to the advantages of the long-range wireless shortcuts introduced into the network as well as the hierarchical division of the NoC. Due to the wireless shortcuts in the WiNoC, the average hop-count between cores is much less compared to that of a mesh of the same size. Hence, as shown in [7] the performance of the WiNoC is much better compared to the wireline mesh NoC. However, similar to the JTEC-SQED scheme, the H-PC codec also adds timing overheads to the wireless links. The encoder design as outlined in subsection 2.2.2 requires a (38, 32) encoding on each 32 bit flit which then are stored until 4 flits are received. All 4 flits are then encoded with 38 parallel (7, 4) Hamming encoders. Hence, the overhead of the H-PC encoder is equal to the delay of one (38, 32) Hamming encoder and one (7, 4) Hamming encoder as all the (7, 4) encoders operate in parallel. The delays of the various stages of the H-PC and JTEC-SQED schemes are shown in Table I. The latency penalty due to the code-rate of (32x4)/(38x7) = 0.48 is also taken into account. In the wireline links however, extra cycles were not required due to the code-rate as the redundant bits could be transferred in the same cycle with additional wires. Fig. 8 shows the overall latency characteristics of the WiNoC and the wireline mesh with and without coding. Due to the low code rate of the H-PC as well as codec overheads the overall latency of the WiNoC with coding is higher than the WiNoC without coding. However, even with coding the latency of the WiNoC is much less compared to that of a wireline mesh NoC without any coding.

The codecs introduce additional hardware components and hence also require silicon area overheads. Table II summarizes the area overheads of each of the coding schemes. The reported area is the area of the codec required per port of the switches or hubs.

V. CONCLUSION

Wireless Network-on-Chip has emerged as one of the many alternative interconnect technologies for future multi-core chips. However, the reliability of on-chip wireless links is much less compared to the wired interconnects. In this work we propose a unified ECC mechanism by which we can restore the reliability of the wireless links to that of the wired interconnects and also reduce energy dissipation on the wired interconnects. It is demonstrated that with such ECC enhanced wireless links on the chip it is possible to achieve lower energy dissipation, lower latency and almost equally reliable on-chip data communication compared to traditional multi-hop wireline NoCs.

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<th>Area (μm²)</th>
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</tr>
<tr>
<td>JTEC-SQED</td>
<td>11055</td>
</tr>
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TABLE II. AREA OVERHEAD OF THE CODEC FOR EACH CODING SCHEME


