ABSTRACT

In the design of high-performance massive multi-core chips, power and heat have become dominant constraints. Increased power consumption can raise chip temperature, which in turn can decrease chip reliability and performance and increase cooling costs. In this paper we demonstrate how small-world Network-on-Chip (NoC) architectures with long-range wireless links and DVFS-enabled wireline links facilitate design of energy and thermally efficient and hence sustainable multi-core chips. Our performance analysis demonstrates that the DVFS-enabled Wireless NoC improves overall energy dissipation by around 60% and reduces the temperature of the hottest node in the network by up to 30% depending on the specific application without incurring any latency penalty over a traditional mesh network.

I. INTRODUCTION

The continuing progress and integration levels in silicon technologies make possible complete end-user systems on a single chip. An important performance limitation of massive multi-core chips designed with traditional network fabrics arises from planar metal interconnect-based multi-hop links, where the data transfer between two distant blocks can cause high latency and power consumption. Increased power consumption will give rise to higher temperature, which in turn can decrease chip reliability and power consumption. Increased power consumption will give rise to higher temperature, which in turn can decrease chip reliability and performance and increase cooling costs. Different approaches for creating low latency, long-range communication channels like optical interconnects, on-chip transmission lines and wireless interconnects have been explored. These emerging interconnect technologies can enable the design of so called small-world on-chip network architectures, where closely spaced cores will communicate through traditional metal wires, but long distance communications will be predominantly achieved through high performance specialized links [1].

One possible innovative and novel approach is to replace multi-hop wireline paths in a NoC by high-bandwidth single-hop long-range wireless links [2] [3]. The on-chip wireless links facilitate design of a small-world NoC by enabling one-hop data transfers between distant nodes. In addition to reducing interconnect delay, eliminating multi-hop long distance wireline communication reduces the energy dissipation as well. However, the overall energy dissipation of the wireless NoC is still dominated by wireline links. As the link utilization varies depending on the on-chip communication patterns, tuning the link bandwidth accurately to follow the traffic requirements opens up possibilities of significant power savings. Dynamic voltage and frequency scaling (DVFS) is a well-known technique that enables adjusting the bandwidth of the interconnects by suitably varying their voltage and frequency levels. Consequently, this will enable power savings and lowering of temperature hotspots in specific regions of the chip. In this work our aim is to show how a small-world NoC architecture with long-range wireless links and DVFS-enabled wireline interconnects lowers the energy dissipation of a multi-core chip, and consequently helps to improve the thermal profile.

II. RELATED WORK

Conventional NoCs use multi-hop packet switched communication. By using virtual express lanes to connect distant cores in the network, it is possible to avoid the router overhead at intermediate nodes, and thereby improve NoC performance in terms of power, latency and throughput [4]. NoCs have been shown to perform better by insertion of long range wireline links following principles of small-world graphs [1].

Designs of small-world based hierarchical wireless NoC architectures were introduced and elaborated in [2] [3]. Recently, the design of a wireless NoC based on CMOS ultra wideband (UWB) technology was proposed [5]. In [6], the feasibility of designing miniature antennas and simple transceivers that operate in the sub-THz frequency range for on-chip wireless communication has been demonstrated. Most of the existing works related to the design of wireless NoC demonstrate its advantages in terms of latency and energy dissipation provided by the wireless channels only. The main emphasis always has been on the characteristics of the wireless links. However, the overall energy dissipation of the wireless NoC can be improved even further if the characteristics of the wireline links are optimized as well depending on their utilization requirements based on the traffic patterns. DVFS is known to be an efficient technique to reduce energy dissipation of interconnection networks. In this paper our aim is to show how a small-world wireless NoC architecture with DVFS-enabled wireline links improves the energy dissipation and thermal profile of a multi-core chip.
III. PROPOSED ARCHITECTURE

Traditionally, a mesh is the most popular NoC architecture due to its simplicity and the regularity of grid structure. However, one of the most important limitations of this architecture is the multi-hop communications between far apart cores, which gives rise to significant latency and energy overheads. To alleviate these shortcomings, long-range and single-hop wireless links are inserted as shortcuts on top of a mesh. It is shown that insertion of long-range wireless shortcuts in a conventional wireline NoC has the potential for bringing significant improvements in performance and energy dissipation [2] [3]. Inserting the long-range links in a conventional wireline mesh reduces the average hop count, and increases the overall connectivity of the NoC. In this wireless mesh (WiMesh), by careful placement of wireless links depending on inter-core distance and traffic patterns we enable savings in latency, energy, and heat dissipation. In addition, by implementing per-link DVFS on wireline links, the DVFS-enabled WiMesh (D-WiMesh) further improves upon savings in energy and heat dissipation, without incurring any latency penalty with respect to the original mesh.

A. Physical Layer Design

Suitable on-chip antennas are necessary to establish the wireless links. It has already been shown that wireless NoCs designed using carbon nanotube (CNT) antennas can outperform conventional wireline counterparts significantly [2]. Antenna characteristics of carbon nanotubes (CNTs) in the THz frequency range have been investigated both theoretically and experimentally [7]. Moreover, these antennas can achieve a bandwidth of around 500 GHz. Thus, antennas operating in the THz/optical frequency range can support very high data rates. Radiation characteristics of multi-walled carbon nanotube (MWCNT) antennas are observed to be in excellent quantitative agreement with traditional radio antenna theory [7], although at much higher frequencies of hundreds of THz. Such nanotube antennas are good candidates for establishing on-chip wireless links and are considered here.

B. Wireless Link Placement

Using CNT antennas, different frequency channels can be assigned to pairs of communicating source and destination nodes [2]. This will require using antenna elements tuned to different frequencies for each pair, thus creating a form of frequency division multiplexing (FDM), creating dedicated channels between a source and destination pair. This is possible by using CNTs of different lengths, which are multiples of the wavelengths of the respective carrier frequencies. High directional gains of these antennas, demonstrated in [7], aid in creating directed channels between source and destination pairs. In [8], 24 continuous wave laser sources of different frequencies are used. Thus, these 24 different frequencies can be assigned to multiple wireless links in the WiMesh in such a way that a single frequency channel is used only once to avoid signal interference on the same frequencies. This enables concurrent use of multi-band channels over the chip. Hence, in this work we assume 24 wireless links each with a single channel for the WiMesh architecture. The placement of the links is dependent upon three main parameters, the number of cores, the number of long range links to be placed, and the traffic distribution. The aim of the wireless link placement is to minimize the hop count of the network. As discussed in [2], we optimize the average hop count weighted by the probability of traffic interactions among the cores. In this way equal importance is attached to both inter-core distance and frequency of communication. A single hop in this work is defined as the path length between a source and destination pair that can be traversed in one clock cycle. Wireless link placement is crucial for optimum performance gain as it establishes high-speed, low-energy interconnects on the network. It is shown in [2] that for placement of wireless links in a NoC, the Simulated Annealing (SA)-based methodology converges to the optimal configuration much faster than the exhaustive search technique. Hence, we adopt a SA based optimization technique for placement of the wireless links in this work to get maximum benefits of using the wireless shortcuts. We also need to ensure that the introduction of wireless shortcuts does not give rise to deadlocks in data exchange. The routing adopted here is a combination of dimension order (X-Y) routing for the nodes without wireless links and South-East routing algorithm for the nodes with wireless shortcuts. This routing algorithm is proven to be deadlock free in [1].

C. Dynamic Voltage and Frequency Scaling

It has already been shown that by introducing wireless links as long-range shortcuts onto a conventional wireline NoC, savings in latency and energy is obtained [2] [3]. By reducing the hop count between largely separated communicating cores, wireless shortcuts have been shown to attract a significant amount of the overall traffic within the network [2]. The amount of traffic detoured is substantial and the low power wireless links enable energy savings. However, the energy dissipation within the network is still dominated by the flits traversing the wireline links. One popular method to reduce energy consumption of these wireline links is to incorporate DVFS. A method for history based link level DVFS was proposed in [9]. In this scheme, every NoC router predicts future traffic patterns based on what was seen in the past. The metric to determine...
whether DVFS should be performed is link utilization. The short term link utilization is characterized by (1).

\[ U_{\text{Short}} = \frac{1}{H} \sum_{i=1}^{H} f_i \]  

(1)

Where, \( H \) is the history window, and \( f_i \) is 1 if a flit traversed the link on the \( i^{th} \) cycle of the history window and a 0 otherwise. The predicted future link utilization, \( U_{\text{Predicted}} \), is an exponential weighted average determined for each link according to (2).

\[ U_{\text{Predicted}} = \frac{W U_{\text{Short}} + U_{\text{Predicted}}}{W + 1} \]  

(2)

Where, \( W \) is the weight given to the short term utilization over the long term utilization. After \( T \) cycles have elapsed, where \( 1/T \) is the maximum allowable switching rate, the router determines whether a given link’s predicted utilization meets a specific threshold. By allowing thresholds at several different levels of \( U_{\text{Predicted}} \), a finer-grain balance between energy savings, due to lowering the voltage and frequency, and latency penalty, due to mispredictions and voltage/frequency transitions, can be obtained.

Voltage regulators are required to step up or step down voltage in order to dynamically adjust voltage, and hence frequency. By following [10], and using on-chip voltage regulators, transition time can be reduced drastically.

Similar to [9], a DVFS algorithm was developed using (1) and (2). After \( T \) cycles, the algorithm determines if DVFS should be performed on the link based on the predicted bandwidth requirements of future traffic. Depending on which threshold was crossed, if any, the router then determines whether or not to tune the voltage and frequency of the link. In order to prevent a direct multi-threshold jump, which would cause high delay, the voltage and frequency can step up once, step down once, or remain unchanged during one voltage/frequency transition. After each adjustment of the voltage/frequency pair on a given link, energy savings and latency penalty was determined. The energy of the link, \( E_{\text{link}} \), was determined by (3).

\[ E_{\text{link}} = \sum_{N_{\text{flits}}} N_{\text{flits}} \cdot E_{\text{flit}} \cdot V_T^2 \]  

(3)

Where \( N_{\text{flits}} \) is the number of flits over the period \( T \), \( E_{\text{flit}} \) is the energy per flit of the link, and \( V_T \) is the DVFS-scaled voltage for the given period. The total energy of the link is summed over all switching

Figure 2: Latency Penalty vs. Switching Window Size of a Link (FFT) periods within the entire simulation period.

Latency penalty due to DVFS is composed of two main factors.

1) A misprediction penalty is caused when the adjusted voltage/frequency pair did not meet the bandwidth requirements of the traffic over the given switching interval. The bandwidth requirement of the link was obtained by viewing the current link utilization over a smaller window whose size was determined as the average latency of a flit in the non-DVFS network. An example of the misprediction penalty can be seen in Fig. 1. Here, each bar represents the link utilization over an N-cycle window. If the bar is higher than the threshold line, the bandwidth requirements of the flits traversed in that window were not met. This results in a latency penalty for the flits in that N-cycle window. This penalty can be considered as worst case, as it assumes that every flit is time-critical, and a processor may be able to progress after the flit arrives.

2) Adjusting the voltage/frequency pair on the link causes a switching penalty. A transition delay of 100ns was accounted for according to [10]. During this transition, we conservatively do not attempt to send any information on the link.

To determine the appropriate switching window, we find the misprediction penalty and switching penalty of a given link. Fig. 2 shows the total latency penalty in the presence of FFT traffic while varying \( T \). The other benchmarks also show the same trend. A small switching window may catch data bursts, which do not represent a long-term trend of the benchmark’s traffic. Consequently, widely varying short-term traffic utilizations, which can be seen in Fig. 1, will cause the voltage/frequency to change often. As seen in Fig. 2, for small switching windows, there is a large penalty due to frequently changing the voltage/frequency pair of the link. As the switching window widens, the switch penalty reduces drastically, while the overhead due to latency penalty increases slowly. A switching window size of \( T = 5000 \) was selected as the benefits of a larger window size beyond that were minimal.

From [9] and [10], appropriate voltage/frequency pairs were obtained. Based on these pairs, required bandwidth thresholds were determined to be
proportional to the scaled voltage/frequency pairs. The values can be seen in Table 1.

### Table 1: Voltage/Frequency/Threshold Combinations

<table>
<thead>
<tr>
<th>Voltage (V)</th>
<th>Frequency (GHz)</th>
<th>Threshold</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>2.5</td>
<td>≥ 0.9</td>
</tr>
<tr>
<td>0.9</td>
<td>2.25</td>
<td>≥ 0.8</td>
</tr>
<tr>
<td>0.8</td>
<td>2.0</td>
<td>≥ 0.7</td>
</tr>
<tr>
<td>0.7</td>
<td>1.75</td>
<td>≥ 0.6</td>
</tr>
<tr>
<td>0.6</td>
<td>1.5</td>
<td>≥ 0.5</td>
</tr>
<tr>
<td>0.5</td>
<td>1.25</td>
<td>&lt; 0.5</td>
</tr>
</tbody>
</table>

From Fig. 3, it can be seen that the link frequency tracks the utilization over an H-cycle window. We scale our voltage/frequency after T cycles have elapsed in order to prevent large latency penalties due to frequency switching. This method will attempt to predict the next T cycles correctly by tracking the utilization of the link over time.

### IV. PERFORMANCE EVALUATION

In this section, we characterize the performance of the proposed WiMesh architecture by incorporating DVFS through detailed full system simulations. We use the GEM5 [11] platform, with Ruby and Garnet for carrying out detailed performance evaluations. The NoC routers are synthesized from a RTL level design using 65nm standard cell libraries from CMP (http://cmp.imag.fr), using Synopsys™ Design Vision. The NoC drivers are driven with a clock of frequency 2.5 GHz. Three SPLASH-2 [12] benchmarks, FFT, RADIX, LU, and the PARSEC benchmark, CANNEAL [13] are considered to study the latency, energy dissipation, and thermal characteristics of WiMesh.

Within the GEM5 platform, the benchmarks are run from beginning to the end, and statistics are obtained at the completion of each benchmark. We consider a system of 64 alpha cores running Linux. The cores are arranged on a 20mm x 20mm die. The width of all wireline links is considered to be the same as the flit size, which is 32.

#### A. Performance Metrics

To characterize the performance of the DVFS-enabled WiMesh we consider three parameters: latency, energy dissipation, and thermal profile.

Latency values were obtained through Garnet output. We consider average network latency per flit as the relevant parameter. The latency penalty caused by DVFS was calculated as described in section III-(c). The energy dissipations of network routers were obtained from the synthesized netlist by running Synopsys™ Prime Power. The energy dissipation of the wireless links were obtained through HSPICE simulations taking into account the specific lengths of each link based on the established connections in the 20mm x 20mm die. Each wireless link can sustain a data rate of 10Gbps [2]. The energy dissipation of each wireless link was found to be .33pJ/bit [2]. Energy savings by enabling DVFS was calculated as described in III-(c).

As temperature is closely related to the energy dissipation of the integrated circuit, the thermal profile depends on the energy dissipation of the NoC, which is quantified in section IV-(c). To quantify the effects of the WiMesh architecture on heat, its thermal profile is evaluated. The temperature profile of the WiMesh and D-WiMesh is obtained by using the HotSpot tool [14]. To further compare the characteristics of the thermal profiles of a particular region in the NoC, another important parameter that needs to be determined is the average communication density given by (4).

\[
\rho_{\text{comm}} = \frac{1}{C} \left[ \sum_{i=1}^{N_{\text{router}}} N_{\text{fr}}/N_{\text{router}} + \sum_{i=1}^{N_{\text{link}}} N_{\text{fl}}/N_{\text{link}} \right]
\]  

Where, \( \rho_{\text{comm}} \) is the average communication density over the region of interest. \( N_{\text{router}} \) is the number of routers in the region of interest, \( N_{\text{link}} \) is the number of links in the region of interest, \( N_{\text{fr}} \) and \( N_{\text{fl}} \) are the number of flits traveled on each router and link in that region respectively, and \( C \) is the total number of cycles executed. As communication density increases, temperature increases.

#### B. Latency Characteristics

In this subsection, we evaluate the performance of the proposed architecture in terms of latency. Fig. 4 shows the latency of the WiMesh and DVFS-enabled WiMesh versus the traditional mesh. As seen in Fig. 4, the reduction in latency of the WiMesh for FFT, RADIX, LU, and CANNEAL traffics are 22.57%, 24.88%, 23.08%, and 23.75%, respectively, compared to a conventional mesh. The latency savings of the WiMesh over the conventional wireline mesh was similar for all of the benchmarks considered. The latency savings is due to the wireless link placement that takes into account interactions among the cores depending on the traffic pattern in addition to the physical distance between them. By taking a wireless long-range link, we have effectively bypassed multiple hops that would have been taken with a traditional mesh-based design. By enabling DVFS on the wireline links of the WiMesh architecture, the latency penalty from dynamic adjustments to the voltage/frequency as well as mispredictions can balance with the latency improvements of the WiMesh architecture. The net
C. Energy Dissipation

In this subsection we evaluate the energy dissipation characteristics of the WiMesh both with and without DVFS, and compare that with the conventional mesh. The total energy of all routers and links in the NoC was determined. The energy savings can be seen in Fig. 5. The total energy/cycle for the mesh running the FFT benchmark is 370 pJ/cycle, where the WiMesh dissipates 262 pJ/cycle. For RADIX traffic, the mesh dissipates 198 pJ/cycle while the WiMesh dissipates 131 pJ/cycle. The LU traffic running on mesh and WiMesh dissipate 196 pJ/cycle and 138 pJ/cycle respectively. Finally, with CANNEAL traffic, the energy per cycle of the mesh and WiMesh were 1211 pJ/cycle and 817 pJ/cycle respectively.

From Fig. 5 it can be seen that by appropriately placing the long-range wireless links according to the traffic pattern, energy savings is obtained. The wireless links handled 33%, 33%, 35%, and 33% of all traffic for the FFT, RADIX, LU, and CANNEAL benchmarks, respectively. This is a significant amount of traffic considering there are only 24 long-range wireless links whereas there are 112 wireline links. As a high amount of traffic is carried by the low power wireless links, the savings in energy dissipation is significant. Conversely, this still suggests that the majority of the traffic travels on the wireline links. To further reduce the energy dissipation of the flits traversing on wireline links, we enabled DVFS on them. From Fig. 5, it can be seen that by dynamically reducing the voltage and frequency of the wireline links in the WiMesh, that we have further reduced the energy dissipation in comparison to the traditional mesh. The D-WiMesh dissipates 151 pJ/cycle, 75 pJ/cycle, 81 pJ/cycle, and 471 pJ/cycle in presence of FFT, RADIX, LU, and CANNEAL traffics respectively.

This corresponds to 59.22%, 62.01%, 58.58%, and 61.11% energy savings for the respective benchmarks over the traditional mesh.

D. Thermal Profile

In this subsection we evaluate the thermal profile of the WiMesh incorporating DVFS. To further understand the thermal profile, we first obtain the communication densities of the WiMesh and traditional mesh architectures in presence of the different traffics. The average communication density, shown in Fig. 6 was determined over the hotspot area of the network for each benchmark to analyze the thermal profile. As can be seen, there is a large reduction in communication density within the hottest area of the chip of the WiMesh. This directly relates to the thermal profile of the chip, as reduction in communication density will produce less heat.

To be more exact, the average link communication densities in WiMesh within the hotspot region of interest were reduced by 83.3%, 79.4%, 75.4%, and 88.65% for the FFT, RADIX, LU, and CANNEAL traffics, respectively, compared to the traditional mesh topology. The long-range links overwhelmingly take a lot of pressure away from the hotspot region by reducing the communication density by a significant amount. Similarly, savings of average router communication densities were 56.4%, 61.3%, 49.7%, and 64.5% for the FFT, RADIX, LU, and CANNEAL traffics, respectively. To relate this communication density to heat, we consider the CANNEAL case, as its communication density is the largest of our benchmarks.

C. Average Communication Density of Hotspot Region
As explained in section IV-(a), we use the HotSpot tool to determine the thermal profile. Fig. 7 depicts the temperature profiles of the conventional wireline mesh, WiMesh, and D-WiMesh in presence of CANNEAL traffic. Within the traditional mesh hotspot, the hottest router was determined to be 74.96°C. This same router within the WiMesh architecture was reduced by 17.24°C, to 57.72°C. This corresponds to a 23% reduction in temperature. This temperature difference directly relates to the large reduction in communication density as mentioned earlier within the hotspot region. With the DVFS-enabled WiMesh, we have further reduced the energy of the wireline links, and the corresponding ports of the routers. By implementing DVFS on top of the WiMesh, we have reduced the same hotspot router an additional 5.32°C over the WiMesh. The hottest spot of the original mesh network has been reduced by 22.56°C, corresponding to a 30.1% temperature decrease in the DVFS-enabled WiMesh. Similarly, the hottest spot of the mesh was reduced by 13.5%, 6.6%, and 6.9% for the FFT, RADIX, and LU traffics respectively. The temperature reduction in CANNEAL is maximum as it has the highest communication density.

V. CONCLUSIONS AND FUTURE WORK

In this paper, we have demonstrated how a small-world DVFS-enabled wireless NoC improves both the energy and thermal profile of a multi-core chip. By adopting a small-world interconnection infrastructure, where long distance communications will be predominantly achieved through high performance specialized single-hop wireless links, communications can be made significantly more energy efficient. The low power and long-range wireless links carry a significant percentage of the overall traffic, and hence we are able to reduce the temperature hotspot regions in the system. To further extend the energy savings, implementing link level DVFS on wireline links, we are able to reduce energy significantly, and hence reduce the overall chip temperature more.

We intend to extend this work by complementing the energy savings at the network level with suitable methodologies to improve the energy and thermal profiles of the computational cores within the DVFS-enabled WiMesh framework. With DVFS implemented both at the network level and processor level larger energy savings and hence, better thermal profile can be realized.

VI. ACKNOWLEDGMENTS

This work was supported in part by the US National Science Foundation (NSF) CAREER grant (CCF-0845504).

REFERENCES