Guest Editors' Introduction: Promises and Challenges of Novel Interconnect Technologies

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COMMERCIAL DESIGNS currently integrate tens to hundreds of embedded functional and storage blocks in a monolithic SoC, and the number is expected to increase significantly in the near future. Specifically, molecular-scale computing will allow additional orders-of-magnitude improvements in device density. The possibility of such high levels of integration in a single chip necessitates the design of high-bandwidth, low-power interconnect architectures.

With the well-known trend of continued CMOS scaling in accordance with Moore's law, it's projected that traditional on-chip interconnect systems will soon be very limited in meeting the performance needs and specifications of ICs and SoCs. This limit stems primarily from global interconnect delays which significantly exceed gate delays. Copper and low-*k* dielectrics have been introduced to decrease the global interconnect delay, but these traditional materials extend the lifetime of conventional interconnect systems only by a few technology generations. According to the *International Technology Roadmap for Semiconductors* (ITRS), material innovation with traditional scaling will no longer satisfy performance requirements over the long term, which will necessitate new interconnect paradigms. In other words, with technology scaling, dependence on traditional materials innovation alone will lead to a brick wall, which only radically different interconnect architectures will enable us to overcome.

The conventional 2D copper-based IC is inherently limited because of the planar structure's geometrical constraints. Innovative interconnect paradigms based on optical technologies, RF and wireless methods, and carbon nanotubes are promising alternatives that may indeed overcome the challenges presented. Although some of these approaches could still be regarded as 2D, they typically offer new degrees of freedom that could have substantial impact on how interconnects are designed and routed, as well as on the delay and power dissipation. In addition to the design and fabrication aspects, other challenges include problems with reliability and development of adequate CAD tools. With technology scaling, the interconnect fabrics will be severely affected by different sources of transient and permanent failures. A big question is how to produce reliable, predictable interconnect architectures from inherently unreliable components. The new interconnect technologies will enable the integration of heterogeneous components (electrical and nonelectrical) in a single SoC. The design of these complex, heterogeneous SoCs will require new simulation and modeling tools.

This special issue highlights recent investigations of various revolutionary interconnect paradigms as to whether they can deliver on the promise of greater integration, high performance, good scalability, and high energy efficiency in future SoCs and various other computing platforms. The selected articles represent a wide range of emerging interconnects, from carbon nanotubes, to optical, RF, and on-chip wireless communications.

"Optical Interconnect for High-End Computer Systems," by Ron Ho et al., discusses the use of silicon photonics technology to design large-scale chip

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arrays, copackaged with a silicon wafer lattice. The authors emphasize the rationale for using optics for multichip packages. Through qualitative discussions, the authors highlight the roles of three important factors—bonding, clock distribution, and device calibration—on the overall system design and testing.

In "Carbon Nanomaterials: The Ideal Interconnect Technology for Next-Generation ICs," Hong Li, Chuan Xu, and Kaustav Banerjee present a comprehensive overview of state-of-the-art carbon nanomaterials—carbon nanotubes (CNTs) and graphene nanoribbons (GNRs), as next-generation interconnect technology. The authors have presented electrical modeling and performance analysis for various CNT- and GNR-based interconnects and established performance benchmarks with respect to conventional copper interconnects. In addition, the authors have highlighted manufacturability issues of CNT- and GNR-based interconnects.

The next article is "Short-Range, Wireless Interconnect within a Computing Chassis: Design Challenges," by Patrick Chiang et al. This article proposes the design of a short-range wireless communication link to be used in a chassis consisting of multiple chips. The authors demonstrate through experimental results carried out within a valid multisocket server that the channel loss, multipath, and electromagnetic interference are tolerable and will not fundamentally limit wireless chassis communications. Operation of a 4-GHz, 500-Mbps, Ultra-Wideband (UWB) prototype transceiver in 90-nm CMOS technology is shown to establish the feasibility of this within-chassis wireless interconnect.

The fourth article, "Wireless Interconnect and the Potential for Carbon Nanotubes" by Alireza Nojeh and Andre Ivanov, explores the possibility of creating an on-chip wireless communication network using CNT antennas. This is a revolutionary concept in which CNT antennas are used to create an intrachip wireless interconnect using optical instead of radio frequencies and thereby significantly reduce the area overhead. Through qualitative discussions and experimental results, the authors demonstrate the optical antenna properties of CNTs. Additionally, the authors discuss the challenges related to controlled fabrication and device-to-device variations for the CNT antennas.

The last article, "Global On-Chip Coordination at Light Speed" by Zheng Li et al., proposes a design of a photonic on-chip network for many-core systems. This article presents a broadcast-based on-chip communication scheme using nanophotonics, which offers low-latency, power-efficient global on-chip coordination for emerging many-core systems and parallel applications. Through extensive simulation-based studies, the authors demonstrate the capabilities of on-chip optical network as a communication infrastructure for massive multicore chips.

According to the ITRS, up to 80% of microprocessor power will be consumed by interconnects in the near future. It is also predicted that in years to come, the energy dissipation per bit for on-chip communication is not scaling down but remaining static. Consequently, it is imperative to seek revolutionary technological innovations to address the performance bottleneck introduced by conventional metal interconnects. Different revolutionary approaches have been proposed for creating low-latency, low-power, and long-range communication channels like optical interconnects, on-chip transmission lines, and wireless interconnects. Although all these emerging methodologies are capable of improving the power and latency characteristics of today's chips, we need extensive investigations to determine their suitability for replacing and/or augmenting existing metal-and-dielectric–based planar interconnection architectures. We hope that some of these novel technologies presented in this special issue will soon secure their respective niches in the design of highly integrated system chips. ■

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