

# Design of Low Power & Reliable Networks on Chip Through Joint Crosstalk Avoidance and Multiple Error Correction Coding

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**Abstract** Network on Chip (NoC) is an enabling methodology of integrating a very high number of intellectual property (IP) blocks in a single System on Chip (SoC). A major challenge that NoC design is expected to face is the intrinsic unreliability of the interconnect infrastructure under technology limitations. Research must address the combination of new device-level defects or error-prone technologies within systems that must deliver high levels of reliability and dependability while satisfying other hard constraints such as low energy consumption. By incorporating novel error correcting codes it is possible to protect the NoC communication fabric against transient errors and at the same time lower the energy dissipation. We propose a novel, simple coding scheme called Crosstalk Avoiding Double Error Correction Code (CADEC). Detailed analysis followed by simulations with three commonly used NoC architectures show that CADEC provides significant energy savings compared to previously proposed crosstalk avoid-

ing single error correcting codes and error-detection/retransmission schemes.

**Keywords** Network on Chip · Crosstalk avoidance · Multiple error correction · Low power · Transient errors · Joint codes

## 1 Introduction and Motivation

Current commercial designs integrate from 10 to 100 embedded functional and storage blocks in a single system-on-chip (SoC), and the number is likely to increase significantly in the near future [2, 13]. Network on chip (NoC) is viewed as a revolutionary methodology to achieve such a high degree of integration in a single SoC. According to the International Technology Roadmap for Semiconductors (ITRS) [10], signal integrity is expected to be an increasingly critical challenge in designing SoCs. The widespread adoption of the NoC paradigm will be possible if it addresses system level signal integrity and reliability issues in addition to easing the design process, and meeting all other constraints and objectives. With shrinking feature size, one of the major factors affecting signal integrity is transient errors, arising due to temporary conditions of the SoC and environmental factors. Among the transient failure mechanisms are crosstalk, electromagnetic interference, alpha particle hits, cosmic radiation, etc. [7, 15]. These failures can alter the behavior of the NoC fabrics and degrade the signal integrity. Providing resilience against such failures is critical for the operation of NoC-based chips. There are many ways to achieve signal integrity. Among different practical methods, use of new materials for device and interconnect, and tight control of device layouts may be adopted in the NoC domain. Here we propose to tackle this

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problem at the design stage. Instead of depending on post-design methods, we propose to incorporate corrective intelligence in the NoC design flow. This will help to reduce the number of post-design iterations. The corrective intelligence can be incorporated into the NoC data stream by adding error control codes to decrease vulnerability to transient errors. The basic operations of NoC infrastructures are governed by on-chip packet-switched networks. As NoCs are built on packet-switching, it is easy to modify the data packets by adding extra bits of coded information in space and time to protect against transient malfunctions.

In the face of increased gate counts, designers are compelled to reduce the power supply voltage to keep energy dissipation to a tolerable limit, thus reducing noise margins [7]. The interconnects become more closely packed and this increases mutual crosstalk effects. Faster switching can also cause ground bounce. The switching current can cause the already low supply voltage to instantaneously go even lower, thus causing timing violations. All these factors can cause transient errors in the ultra deep submicron (UDSM) era [7]. Crosstalk is a prominent source of transient malfunction in NoC interconnects. Crosstalk avoidance coding (CAC) schemes are effective ways of reducing the worst-case switching capacitance of a wire by ensuring that a transition from one codeword to another does not cause adjacent wires to switch in opposite directions. Though CACs are effective in reducing mutual inter-wire coupling capacitance, they do not protect against any other transient errors. To make the system robust, in addition to CAC we need to incorporate forward error-correction coding (FEC) into the NoC data stream. Among different FECs, single error correcting codes (SECs) are the simplest to implement. But aggressive supply-voltage scaling and increases in deep sub-micron noise in future-generation NoCs will prevent SECs from satisfying reliability requirements. Hence, we investigate performance of joint CAC and multiple error correcting codes (MECs) in NoC fabrics. The main contributions of this work are the design of a novel but simple joint CAC/MEC mechanism, and the establishment of a performance benchmark for this scheme with respect to other existing coding methods.

## 2 Related Work

In recent years, there has been an evolving effort in developing on-chip networks to integrate increasingly large number of functional cores in a single die [2, 13]. But even before the advent of the NoC paradigm, different research groups investigated various coding schemes to enhance the reliability of bus-based systems. In [32] the authors proposed to employ data encoding to eliminate crosstalk delay within a bus. They presented a detailed analysis of

the self-shielding codes and established fundamental theoretical limits on the performance of codes with and without memory. In [25], the authors provided a comprehensive study of the usefulness of error correcting codes to reduce the crosstalk-induced bus delay (CIBD), and proved that Dual Rail codes perform better than Hamming codes. The authors of [25] used single error correcting codes (SECs) to minimize crosstalk. These codes are not as efficient as CACs to handle crosstalk related issues. In addition, different low-power coding (LPC) techniques have been proposed to reduce power consumption of on-chip buses [31]. But these LPCs aim at reducing only the self-transition in a wire. According to [11], the principal limitation of the applicability of the LPCs is that, due to higher power dissipation in the codec blocks, these codes are energy efficient only if the length of the wire segment exceeds a certain limit. In [30] the authors presented a unified framework for applying coding for systems on chips (SoCs), but targeted principally for bus-based systems.

In [4, 5], performance of single error correcting and multiple error detecting Hamming codes and cyclic codes in an AMBA bus-based system has been discussed. The energy efficiency and the area overhead of the codecs have also been discussed. These papers conclude that error detection followed by retransmission is more energy efficient than forward error correction (FEC) schemes. Error resiliency in NoC fabrics and the trade-offs involved in various error recovery schemes are discussed in [16]. In this work, the authors investigated performances of simple error detection codes like parity or cyclic redundancy check codes and single error-correcting, multiple error-detecting Hamming codes in NoC fabrics. The basic principle of this work is similar to that of [5]: the receiver corrects only a single bit error in a flow-control-unit (flit), but for more than one error, it requests retransmission from the sender. As mentioned in the concluding remarks of [5], in the ultra deep submicron (UDSM) domain communication energy will overcome computation energy. Retransmission will give rise to multiple communications over the same link and hence ultimately will not be very energy efficient. Moreover retransmission will introduce significant communication latency. In systems dominated by retransmission some additional error correction mechanisms for the control signals need to be incorporated also. Moreover, these codes do not have any crosstalk avoidance characteristics, which are absolutely necessary in the deep submicron (DSM) technology nodes. The role of communication infrastructure of NoCs on energy dissipation is discussed in [18]. Different strategies for power management for NoCs, such as power-aware on-off networks [28], and dynamic voltage scaling [27] have been addressed previously. Application of CAC and joint CAC/SEC in NoCs is also discussed in [17, 19, 20]. In this work we propose a novel joint CAC/MEC

and compare and contrast its performance in NoC architectures with other existing coding schemes.

### 3 Data Coding in NoC Links

The common characteristic of NoC architectures is that the functional IP blocks communicate with each other via intelligent switches. The data communication between IP's in a NoC takes place in the form of packets routed through a wormhole switching mechanism. The packets are broken down into fixed length flow control units or flits. The switch blocks need to store only a few flits [6, 18]. The header flits carry the relevant routing information. Consequently header decoding enables the establishment of a path that the subsequent payload flits simply follow in a pipelined fashion. The transmitted flits are encoded to guard against possible transient errors.

The incorporation of CACs reduces the mutual switching capacitance of the inter-switch wire segments. Though this helps in reducing the energy dissipation in communication, the energy reduction is only linear with the capacitance decrease. On the other hand, incorporation of error correction codes makes the system more robust, so that the voltage level driving the system can be reduced without compromising bit error rates. This makes joint crosstalk-avoidance and error correction codes more suitable for lowering the energy dissipation of on-chip communication infrastructures.

There are a few joint crosstalk avoidance and single error correction codes (CAC/SEC) proposed by different research groups. Among these joint codes, the Dual Rail (DR) Code [23, 24] or Duplicate Add Parity (DAP) [30], Boundary Shift Code (BSC) [22] and Modified Dual Rail Code (MDR) [26] reduce the switching capacitance associated with crosstalk from  $(1+4\lambda)C_L$  to  $(1+2\lambda)C_L$  [29], where  $\lambda$  is the ratio of the coupling capacitance to the bulk capacitance and  $C_L$  is the load capacitance, including the self-capacitance of the wire.

However, due to intensive integration and device shrinkage in the UDMS era, single error correction will not be sufficient to protect against different transient malfunctions. Hence there is a need for multiple error correction schemes. We propose a novel, simple joint crosstalk avoidance and double error correction scheme called crosstalk avoiding double error correction code (CADEC). We investigate the performance of CADEC in comparison with the various existing joint CAC/SEC schemes in different NoC architectures. One point worth noting here is that, according to [4, 5], error detection followed by retransmission is a more energy efficient scheme than the error correction. To establish the performance benchmark for the CADEC scheme, we compare its

performance with error detection (ED) codes also. All the error correcting schemes considered here are enhanced with a retransmission mechanism which is activated when the number of errors in the flit exceeds its correction capability. With increase in the correction capability of a code the probability of retransmission will reduce significantly. For the sake of fair comparison, the same retransmission mechanism is considered across all codes namely, switch-to-switch flit level retransmission (s2sf) [16]. As suggested in [16], an end-to-end retransmission mechanism can also be adopted. But as our emphasis is on characterizing the coding schemes it is sufficient to assume a single retransmission method.

Below we explain the basic principles of all the coding schemes considered in this work.

#### 3.1 DAP and MDR Schemes

The Duplicate Add Parity (DAP) scheme achieves joint crosstalk avoidance and single error correction capability by duplicating each bit of the  $n$ -bit flit and placing the copies adjacent to each other to avoid crosstalk, and by also computing a parity bit from the initial bits to enable single error correction. Thus, the encoded flit becomes  $2n+1$  bits wide [23, 30]. Modified Dual Rail (MDR) code is a simple modification of the DR/DAP scheme, where a second copy of the parity bit is transmitted to guard against crosstalk on the parity bit itself [26]. Thus, the MDR encoded flit is  $2n+2$  bits wide. The encoder and decoder of the DAP scheme are shown in Fig. 1. The MDR scheme is very similar and therefore is not shown separately.

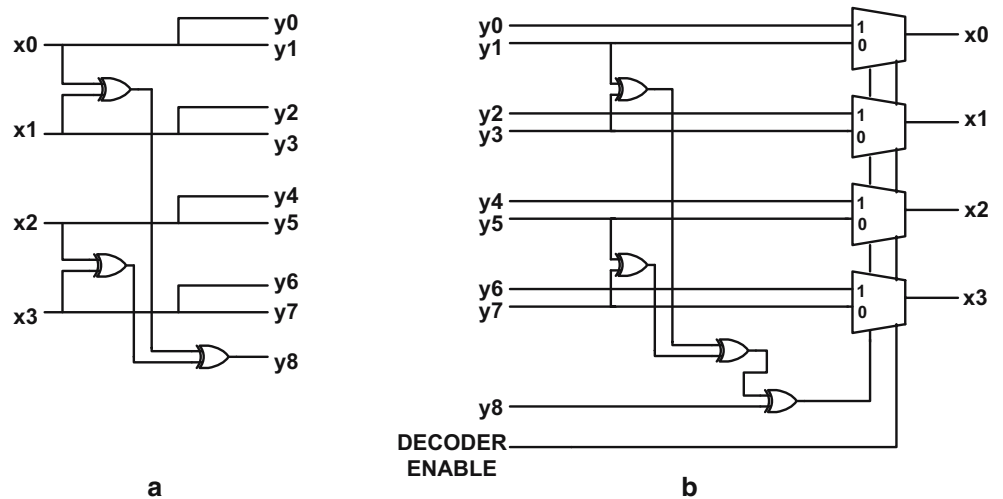
#### 3.2 BSC Scheme

Boundary Shift Coding (BSC) is achieved by avoiding a shared boundary between two successive code words [22]. The scheme duplicates each bit and computes an overall parity, and then each alternate code word is given a cyclic shift in a way that appends the parity bit to either the right or the left of the flit after duplication. The decoding mechanism is the same as in DAP, after carefully extracting the parity bit from the flit depending on whether it is the rightmost or the leftmost bit of the flit. The encoder and decoder for the BSC scheme are shown in Fig. 2.

#### 3.3 Error Detection Code—ED

This scheme implements Hamming code for error detection and retransmits if the scheme detects that the flit is in error [4]. As an example, the (38, 32) shortened Hamming code implemented for a 32 bit wide flit can reliably detect up to two errors in the flit. The ED scheme only detects the errors; on detection of any error pattern, it sends an automatic repeat request (ARQ) signal for retransmission of the flit. The

**Fig. 1** a DAP encoder; b DAP decoder



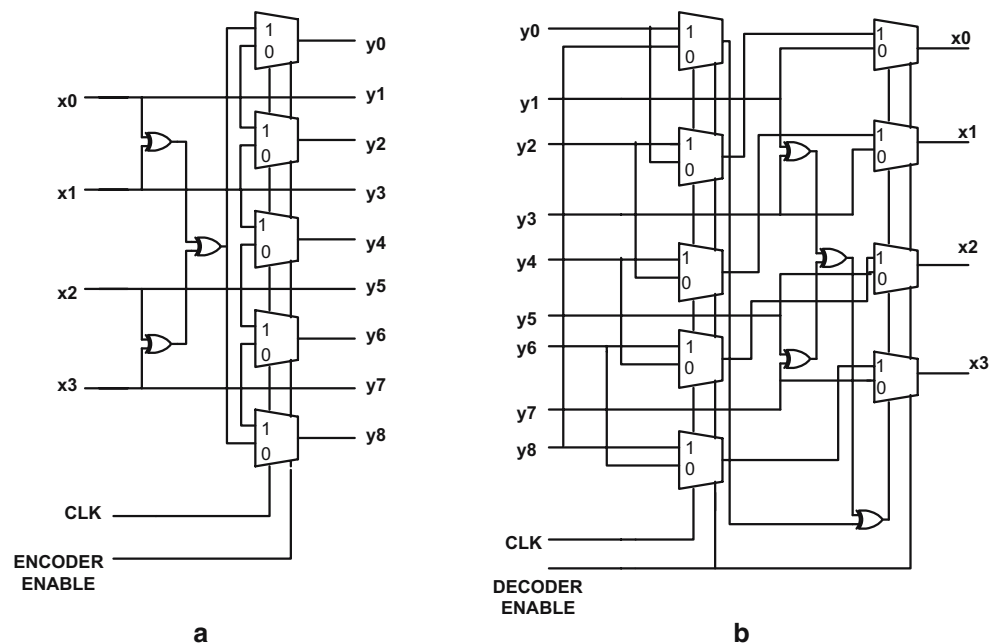
encoder is essentially only a (38, 32) Hamming encoding block. The decoder is also a standard syndrome decoder for the Hamming encoded flit. Evidently, this scheme does not have any crosstalk avoidance properties.

### 3.4 Crosstalk Avoiding Double Error Correction Scheme

Compared with Hamming codes, standard double error correction codes like BCH codes are computationally complex, and therefore are not very efficient from the perspective of energy reduction and area cost. In this work, we design a novel scheme which is capable of joint crosstalk avoidance and double error correction. We call this scheme CADEC coding. The encoder and decoder for the CADEC scheme are described in the following subsections.

*Encoder* The encoder is a simple combination of Hamming coding followed by DAP or BSC encoding to provide protection against crosstalk. As shown in Fig. 4a, the incoming 32-bit flit is first encoded using a standard (38, 32) shortened Hamming code, then each bit of the 38-bit Hamming codeword is duplicated, and an overall parity calculated from one Hamming copy is appended. The (38, 32) Hamming code has a Hamming distance of 3 between adjacent code words. On duplication this becomes 6 and after adding the extra parity bit this distance becomes 7. A Hamming distance of 7 enables triple error correction, but at a somewhat higher complexity cost than the double-error correcting schemes considered here. Consequently, as a first step we considered only the double error correction capability. The extra parity bit, which is a part of DAP or

**Fig. 2** a BSC Encoder; b BSC decoder



BSC schemes, is added to make the decoding process very energy efficient as explained below.

*Decoder* The decoding procedure for the CADEC encoded flit can be explained with the help of the flow diagram shown in Fig. 3. The decoding algorithm consists of the following simple steps:

1. The parity bits of the individual Hamming copies are calculated and compared with the sent parity;
2. If these two parities obtained in step 1 differ, then the copy whose parity matches with the transmitted parity is selected as the output copy of the first stage.
3. If the two parities are equal, then any one copy is sent forward for syndrome detection.
4. If the syndrome obtained for this copy is zero then this copy is selected as the output of the first stage. Otherwise, the alternate copy is selected.
5. The output of the first stage is sent for (38, 32) single error correcting Hamming decoding, finally producing the decoded CADEC output.

The circuit implementing the decoder is schematically shown in Fig. 4(b).

The use of the DAP or BSC parity bit effectively makes the decoder more energy efficient, compared to a scheme without the parity bit, which always requires a syndrome to be computed on both copies.

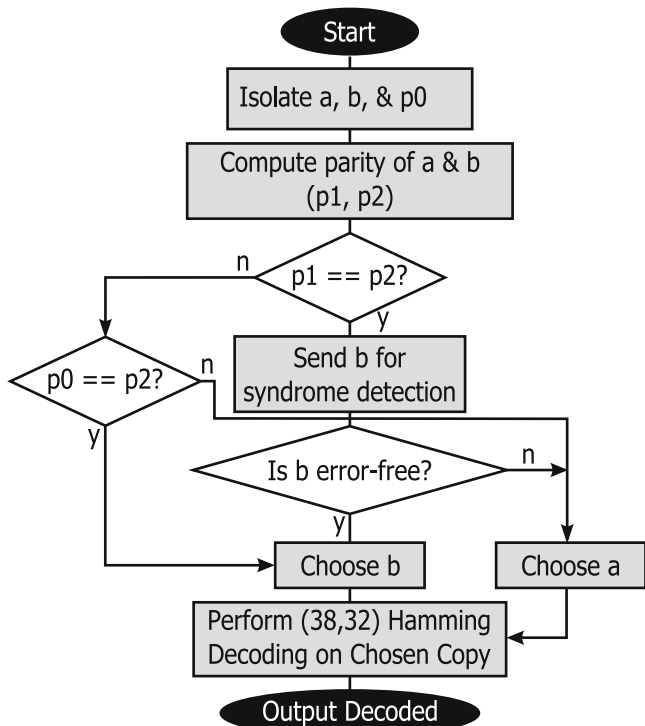


Fig. 3 Decoding Algorithm for the CADEC scheme

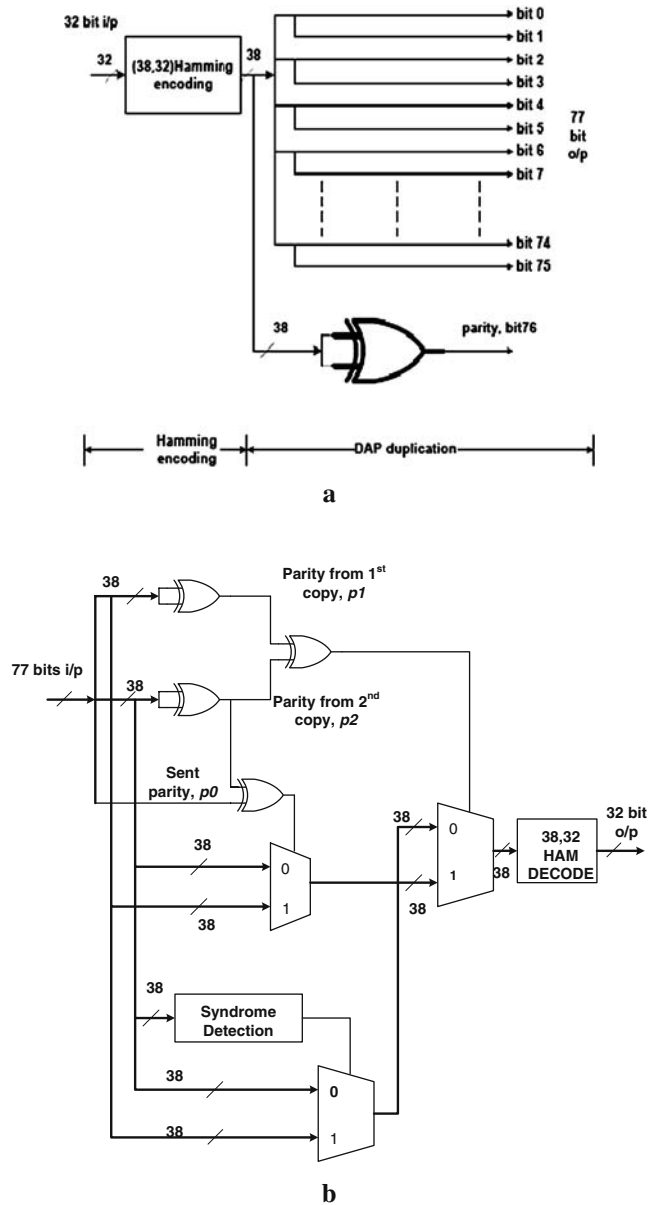


Fig. 4 a CADEC encoder. b CADEC decoder

When the parity bits generated from individual Hamming copies fail to match, the syndrome computing block need not be used at all, thus on average making the overall decoding process more energy efficient. This situation arises when there is single error in either one of the two Hamming copies, which, generally, will be the more probable case. We note that the circuit diagram of Fig. 4 and the flowchart of Fig. 3 show only the logic for double error correction. To simultaneously detect triple or quadruple errors, one additional syndrome computation step must be performed on the copy selected for the final stage; if that copy has a non-zero syndrome, then there are three or more errors in the codeword, and an ARQ request to retransmit the flit should be sent.

### 4 Probability of Undetected Error

In the DSM NoC paradigm, reliability and energy dissipation cannot be decoupled. Enhancing reliability by performing coding invariably increases the energy overhead due to the codec blocks and redundant wires. But due to increased reliability, the voltage level driving the interconnect wires can be reduced without increasing the probability of residual word error, as the reduction in noise margin can be compensated by the increased error resilience [5, 30]. Considerable energy savings can be achieved by reducing the voltage level on the interconnects, since the energy dissipation depends on the voltage squared.

To quantify these gains, consider a Gaussian distributed noise voltage  $V_N$  with variance  $\sigma_N^2$  which models the cumulative effect of all the transient DSM noise sources as mentioned before. This gives the probability of bit error,  $\varepsilon$ , also called the bit error rate (BER) as

$$\varepsilon = Q\left(\frac{V_{dd}}{2\sigma_N}\right), \tag{1}$$

where the  $Q$ -function is given by

$$Q(x) = \frac{1}{\sqrt{2\pi}} \int_x^\infty e^{-\frac{y^2}{2}} dy. \tag{2}$$

The word error probability is a function of the channel BER  $\varepsilon$ . If  $P_{unc}(\varepsilon)$  is the probability of word error in the uncoded case and  $P_{ecc}(\varepsilon)$  is the residual probability of word error with error control coding, then it is desirable that  $P_{ecc}(\varepsilon) \leq P_{unc}(\varepsilon)$ . Using Eq. 1, we can reduce the supply voltage in presence of coding to  $\widehat{V}_{dd}$ , given by

$$\widehat{V}_{dd} = V_{dd} \frac{Q^{-1}(\widehat{\varepsilon})}{Q^{-1}(\varepsilon)}. \tag{3}$$

In (3),  $V_{dd}$  is the nominal supply voltage in the absence of any coding. To compute  $\widehat{V}_{dd}$  for various schemes we find the residual word error probability for each of the schemes investigated in this paper.

#### 4.1 Probability of Undetected Error for ED

As pointed out in [12], any  $(n, k)$  linear code can detect  $2^n - 2^k$  error patterns of length  $n$ . The probability of undetected error for any  $(n, k)$  linear code can be computed from the weight distribution polynomial of the code,  $A(z)$ , given by

$$A(z) = A_0 + A_1z + \dots + A_nz^n, \tag{4}$$

where  $A_k$  is the number of codewords with weight (i.e., the number of 1s in the codeword) equal to  $k$ . The dual of the

linear code also has an associated weight distribution,  $B(z)$ , given by

$$B(z) = B_0 + B_1z + \dots + B_nz^n. \tag{5}$$

The weight distribution of the original code and its dual code are related by [12, 14]

$$A(z) = 2^{-(n-k)}(1+z)^n B\left(\frac{1-z}{1+z}\right). \tag{6}$$

The probability of undetected word error  $P_{ED}(\varepsilon)$  for an error detection scheme using a linear code with dual weight distribution  $B(z)$  is [12]

$$P_{ED}(\varepsilon) = 2^{-(n-k)}B(1-2\varepsilon) - (1-\varepsilon)^n, \tag{7}$$

where  $B(1-2\varepsilon)$  is given by

$$B(1-2\varepsilon) = \sum_{i=0}^n B_i(1-2\varepsilon)^i. \tag{8}$$

The ED scheme proposed in [4] uses the (38, 32) shortened Hamming code for error detection, so the coefficients  $B_i$  in Eq. 8 are obtained by using the H-matrix of that code. Using Eq. 7, the probability of undetected error for the ED code, for small values of BER  $\varepsilon$ , turns out to be

$$P_{ED}(\varepsilon) = (n-k)\varepsilon^2 \tag{9}$$

where  $n=38$  and  $k=32$  for the (38,32) shortened Hamming code.

#### 4.2 Probability of Undetected Error for DAP, BSC and MDR

The DAP coding scheme can correct all single error patterns and some multiple errors, which are taken into account while calculating the probability of undetected error. Let the original uncoded flit consist of  $k$  bits (we assume  $k=32$  here). This makes the length of the DAP encoded flit to be  $(2k+1)$  bits. Correct decoding can happen under two circumstances as discussed below:

1. The parity bit is error-free and one copy of the flit has no errors. The other copy in this case can have any number of erroneous bits. However, the parity has to be regenerated at the decoder only from the copy that is error-free. So, this possibility is not interchangeable between the two copies.
2. The other possibility for correct decoding is when the parity bit is in error. Then, if the  $(k+1)$  bits consisting

of the copy from which the parity is regenerated and the sent parity have an odd number of errors, then the regenerated parity will not match the sent parity and the other copy which is error-free will be selected.

These two cases jointly give the set of cases where correct detection is possible, whose complement is the set of undetected errors. The probability of the set of undetected errors as computed in [30] is given by

$$P_{DAP}(\varepsilon) = 1 - \sum_{i=0}^k \binom{k}{i} \varepsilon^i (1 - \varepsilon)^{2k-1+i} - \sum_{i=0}^{\frac{k}{2}} \binom{2k+1}{2i+1} \varepsilon^{2i+1} (1 - \varepsilon)^{2k-2i}. \tag{10}$$

This can be simplified to the following expression for small values of  $\varepsilon$

$$P_{DAP}(\varepsilon) = \frac{3k(k+1)}{2} \varepsilon^2. \tag{11}$$

BSC and MDR, which perform the decoding following an essentially similar principle, have the same probability of word error as DAP.

### 4.3 Probability of Undetected Error for CADEC

The probability of correct decoding can be found by considering each of the cases where the decoder can correctly decode flits despite errors. The cases where the decoder can correctly decode words with more than two errors also need to be considered. The complement of the set of correctly decoded words constitutes the set of undetected errors. This probability is given by  $P_{CADEC}(\varepsilon)$ . So, we have the relation:

$$P_{CADEC}(\varepsilon) = 1 - P_{correct}. \tag{12}$$

In the following derivation, the width of the original flit is denoted by  $k$ , where  $k$  is 32, which is first Hamming coded to 38 bits, denoted by  $n$ . Each bit of the  $n$ -bit Hamming codeword is duplicated and an overall parity bit is appended. All possibilities of correct decoding are broadly divided into three categories:

1. *Error-free transmitted parity bit:*

One of the copies has no error while the other has anywhere from zero to all bits in error. This can be correctly decoded similarly as in the DAP scheme which is integrated into the novel CADEC scheme.

2. *Single bit error in each copy:*

There is a single error in both copies, irrespective of the parity-bit being in error or not.

3. *Erroneous transmitted parity bit: There are multiple cases under this scenario*

- no errors in either copy
- up to one error in one copy and an even number of errors in the other starting from 2 to  $n$  errors
- a single error in one copy and an odd number of errors in the other.

The complete probability of correct decoding,  $P_{correct}$  is given by the sum of the probabilities corresponding to the above mutually exclusive cases. In the limit of small channel BER  $\varepsilon$ , this can be expressed as

$$P_{correct} = 1 - n^2(n-4)\varepsilon^3. \tag{13}$$

From Eqs. 12 and 13, the word error probability is

$$P_{CADEC}(\varepsilon) = n^2(n-4)\varepsilon^3. \tag{14}$$

Using Eq. 3, along with Eqs. 9, 11, and 14 for the undetected word error probabilities for the different coding schemes, the tolerable voltage swing reduction can be computed against varying values of BER  $\varepsilon$ . The plot of voltage swing versus BER is shown in Fig. 5. The nominal voltage at the 130 nm technology node is assumed to be  $V_{dd}=1.2$  V.

As can be seen from Fig. 5, the voltage swing is lower than the nominal voltage for all the coding schemes. The CADEC scheme provides maximum voltage reduction as it can correct and also detect more errors than the others. For the purpose of simulations the voltage swings for different coding schemes corresponding to the channel BER of  $10^{-20}$  [30] are used later in the paper.

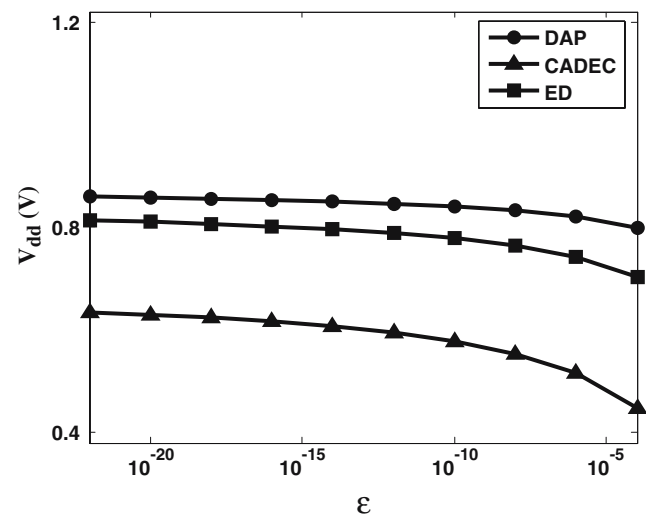


Fig. 5 Variation of achievable voltage swing with bit error rate for different coding schemes

## 5 Energy Dissipation in a NoC Interconnect

When flits travel between switches on the interconnection network, both the inter-switch wires and the logic gates in the switches toggle, resulting in energy dissipation. Furthermore, flits will need to traverse multiple hops to reach their destinations. To determine the energy efficiency of our proposed scheme, we need to determine the energy dissipated in each interconnect and switch hop. The energy per flit per hop is given by the sum

$$E_{\text{hop}} = E_{\text{switch}} + E_{\text{interconnect}}. \quad (15)$$

The energy dissipated in transporting a flit through  $h$  hops can be calculated as

$$E_{\text{flit}} = \sum_{j=1}^h E_{\text{hop},j}. \quad (16)$$

In the presence of coding, the energy dissipated in each hop will be given by

$$E_{\text{hop},j} = E_{\text{switch},j} + E_{\text{codec},j} + E_{\text{interconnect},j}. \quad (17)$$

In order to quantify the energy dissipation profile for a NoC interconnect architecture, we determined the energy dissipated in each switch,  $E_{\text{switch}}$ , and each codec,  $E_{\text{codec}}$  by running Synopsys™ Prime Power on the gate-level netlist of the switch and the codec blocks. Our energy estimation methodology involved feeding a large set of data patterns to the switch and codec blocks. Through functional simulation using Synopsys Prime Power, the average values for the activity factors were determined. To determine the interconnect energy  $E_{\text{interconnect}}$ , the capacitance of each interconnect stage was calculated taking into account the specific layout of each topology [8, 9]. In presence of coding the effective coupling component of this capacitance is however reduced [17]. Thus, in addition to the voltage reduction due to increased reliability, the effective wire capacitance is also reduced. These two factors together contribute to reduce the energy dissipation of the inter-switch wire segments.

Messages can be injected by each IP into the network following different stochastic distributions. In our experiments the traffic injected by the functional IP blocks followed Poisson and self-similar distributions [18]. In the past, a Poisson distributed injection rate was frequently used when characterizing performance of multiprocessor platforms [21]. However the self-similar distribution was found to be a better match to real world SoC scenarios [1].

As will be demonstrated later, the energy savings trend due to coding does not depend strongly on any particular injection pattern.

## 6 Expected Energy Dissipation in Presence of Errors

The schemes investigated here implement corrective intelligence either in the form of joint crosstalk avoidance and forward error correction or error detection followed by retransmission. In the error detection (ED) scheme, whenever an error is detected, the receiving switch asks for retransmission from the previous one. In contrast, the joint crosstalk avoidance and single/multiple error correcting codes ask for retransmission only when the number of errors in a flit exceeds their correction capability. An interesting study is to compare the expected energy dissipation per bit for each of the schemes, given that there is an error in the flit when it is transmitted for the first time. In the following derivations the coded flit length  $m$  is assumed to be 38 for the ED scheme, 65 for DAP, BSC and MDR, and 77 for CADEC.

The retransmission mechanism used for each of the schemes to avoid data loss, is a switch-to-switch, flit level retransmission. If the number of errors in a flit is more than the correction capability of the coding scheme then an automatic repeat request (ARQ) is sent and the erroneous flit is retransmitted. The ED scheme sends ARQ in presence of even a single error. This necessitates adequate buffering at the switches for the flits already transmitted. So, there is an additional energy expenditure associated with the retransmission buffers [16]. The energy dissipation associated with the ARQ signal needs to be considered as well.

### 6.1 Error Detect and Retransmit Scheme-ED

The probability of the flit having an error in the first transmission is given by the following equation, in which the last equality assumes small BER  $\varepsilon$ :

$$P_{\text{error}} = P(\geq 1) = 1 - (1 - \varepsilon)^m = m\varepsilon. \quad (18)$$

Let the event that there is an error in the first transmission be  $B$ , and the event that the  $i$ th transmission is the first error-free transmission after  $i-1$  erroneous transmissions be  $A$ . Then the conditional probability for event  $A$  given event  $B$  has occurred can be computed as

$$P(A/B) = \frac{P(A \cap B)}{P(B)}. \quad (19)$$

As  $A$  is the event that the first  $(i-1)$  transmissions have errors and  $B$  is the event that the very first transmission has

at least a single error we can observe that event  $A$  implies event  $B$ . Thus we may say that  $A \cap B$  equals only  $A$ . Now, the probability of  $i$  repeated transmissions is given by the probability of  $i-1$  transmissions with at least one error and the  $i$ th transmission without any error, which is  $[P(\geq 1)]^{i-1}(1 - P(\geq 1))$ . So, the conditional probability of  $i$  repeated transmissions given an error in the first transmission is

$$P_i = P(A/B) = \frac{[P(\geq 1)]^{i-1}(1 - P(\geq 1))}{P_{\text{error}}}. \tag{20}$$

Hence the expected energy dissipation is given by the following infinite sum, which accounts for all possible transmissions:

$$Ex[E_{\text{bit},ED}/\text{Error}] = \sum_{i=2}^{\infty} P_i \cdot i \cdot E_{ED}. \tag{21}$$

In Eq. 21, the number of transmissions  $i$  starts from 2 as that is the least number of transmissions needed if the first transmission always has an error, and  $E_{ED} = E_{\text{bit},ED} + E_{\text{bit},\text{buf}} + E_{\text{ARQ}}$ . Here,  $E_{\text{bit},ED}$  is the energy dissipated per bit in a inter-switch link in case of the sole ED scheme. The energy factor also includes the energy per bit for the buffer storage,  $E_{\text{bit},\text{buf}}$  and the energy dissipation for the ARQ bit,  $E_{\text{ARQ}}$ . Thus  $i \cdot E_{ED}$  is the energy dissipated per bit in  $i$  repeated transmissions for the ED scheme. This gives the expected energy dissipation for the ED scheme as

$$Ex[E_{\text{bit},ED}/\text{Error}] = \frac{(2 - m\varepsilon)}{(1 - m\varepsilon)} E_{ED}, \tag{22}$$

where  $m$  is the total number of bits in the coded flit. For small  $\varepsilon$  the above equation simplifies to

$$Ex[E_{\text{bit},ED}/\text{Error}] = [2 + m\varepsilon] E_{ED}. \tag{23}$$

It is evident from Eq. 23 that the expected value of energy dissipation in the ED scheme is more than twice that of a single transmission in presence of errors.

### 6.2 DAP, BSC and MDR Coding Schemes

If the DAP, BSC and MDR schemes were enhanced using a retransmission mechanism, then we would expect the energy dissipation to depend on the retransmission probability. The difference between the joint CAC/SEC schemes and the ED scheme is that the joint code will send an ARQ only when there is more than one error in the flit. For any single error the schemes will correct the flit on the fly. Once again, let  $A$  be the event that there are  $i-1$  transmissions with more than one error, which necessitated retransmission for  $i-1$  times, while the last  $i$ th transmission has one or less errors. Also, let  $B$  be the event that the first transmission had at least one error. As in

the case of the ED scheme, we are interested in determining  $P(A/B)$ . As before,  $A \cap B$  as  $A$  is a subset of  $B$ . The conditional probability of having  $i > 1$  repeated transmissions, given an error in the first transmission, follows from (20) and is given by

$$P_i = \frac{P(\geq 2)^{i-1} P(< 2)}{P_{\text{error}}}. \tag{24}$$

Here  $P_{\text{error}}$  is obtained from (19),  $P(< 2)$  is the probability of having less than two erroneous bits in the flit, and  $P(\geq 2)$  is the probability of having two or more errors in the flit which is given by  $1 - P(< 2)$ . Now, for  $i=1$ , the flit had exactly one error and hence was correctable; this probability is given by

$$P_{i=1} = \frac{P(1)}{P_{\text{error}}} = \frac{m\varepsilon(1 - \varepsilon)^{m-1}}{m\varepsilon} \approx 1 - (m - 1)\varepsilon \tag{25}$$

The expected value of the energy dissipation is given by the following sum similar to (22)

$$Ex[E_{\text{bit},DAP}/\text{Error}] = \sum_{i=1}^{\infty} P_i \cdot i \cdot E_{DAP}, \tag{26}$$

where  $E_{DAP} = E_{\text{bit},DAP} + E_{\text{bit},\text{buf}} + E_{\text{ARQ}}$  and  $E_{\text{bit},DAP}$  is the energy dissipated per bit in a inter-switch link in case of the DAP scheme. As before, the retransmission buffer energy and the ARQ energy are also included. Equation 26 can be simplified for small values of  $\varepsilon$  as

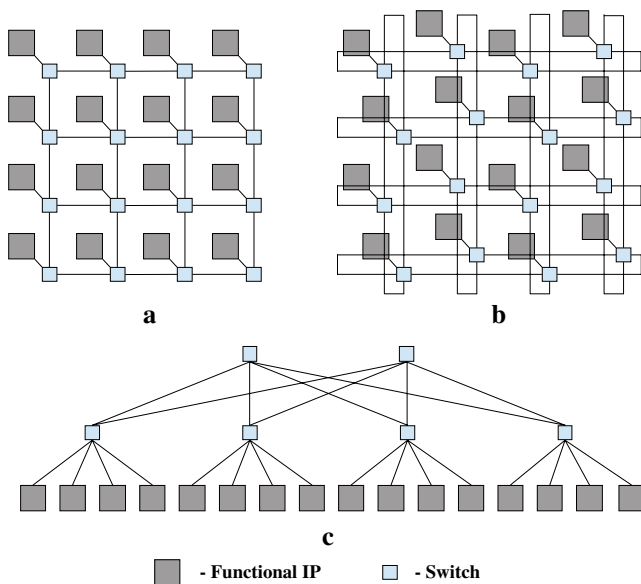
$$Ex[E_{\text{bit},DAP}/\text{Error}] = \left[ 1 + \frac{m(m - 1)^2}{4} \varepsilon^3 \right] E_{DAP}. \tag{27}$$

Equation 27 also gives the expected value of energy dissipation per bit (given an initial error) for BSC and MDR, since they have the same error correction capability as DAP. From Eq. 27, the expected energy dissipation per bit when an error has occurred is less in the case of DAP, BSC or MDR codes than in the case of ED, as they send an ARQ only when there is more than a single error which happens less often than a single error occurring in the transmitted flit.

### 6.3 CADEC Scheme

In CADEC, the expected energy per bit will be less than in ED, as CADEC retransmits only when there are three or more errors compared to ED which retransmits even when there is a single error.

For CADEC, the event  $A$  will be  $i-1$  transmissions with more than two errors and the last transmission with two or less errors. The event  $B$  as before will be the case when the first transmission is in error. Following similar arguments as in the case of ED and DAP,  $A \cap B = A$ . Hence, the conditional



**Fig. 6** NoC architectures **a** MESH **b** FOLDED-TORUS **c** BUTTERFLY-FAT-TREE (BFT)

probability of  $i$  repeated transmissions, where  $i > 1$ , given that the first transmission has an error, is given by

$$P_i = \frac{P(\geq 3)^{i-1} P(< 3)}{P_{error}}, \tag{28}$$

where  $P(< 3)$  is the probability of having 0, 1 or 2 errors in the flit and  $P(\geq 3)$  is the probability of having more than two errors and equals  $1 - P(< 3)$ .

However, if the first transmission has two or less errors then there will be no retransmissions and this event has the probability

$$P_{i=1} = \frac{P(1)}{P_{error}} + \frac{P(2)}{P_{error}} \approx 1 - \frac{(m-1)}{2} \varepsilon, \tag{29}$$

where  $m$  is the number of bits in the coded flit.

Similar to the other schemes the expected value of the energy dissipation in this case is given by

$$Ex[E_{bit,CADEC}/Error] = \sum_{i=1}^{\infty} P_i \cdot i \cdot E_{CADEC} \tag{30}$$

where  $E_{CADEC} = E_{bit,CADEC} + E_{bit,buf} + E_{ARQ}$  and  $E_{bit,CADEC}$  is the energy dissipation per bit for the CADEC scheme. The energy dissipation per bit for the retransmission buffer,  $E_{bit,buf}$  and that for the ARQ bit,  $E_{ARQ}$  are also considered in Eq. 30.

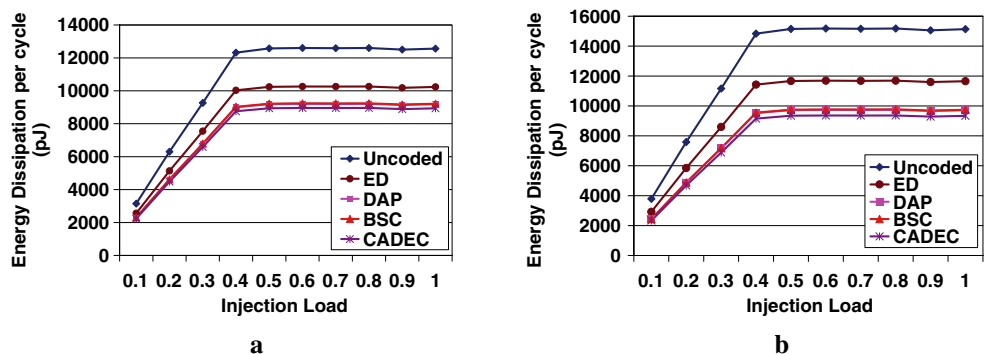
The final expected value of the energy dissipation given there is an error in the flit in presence of CADEC coding simplifies (in the limit of small  $\varepsilon$ ) to

$$Ex[E_{bit,CADEC}/Error] = \left[ 1 - \frac{(m-1)}{2} \varepsilon \right] E_{bit,CADEC} \tag{31}$$

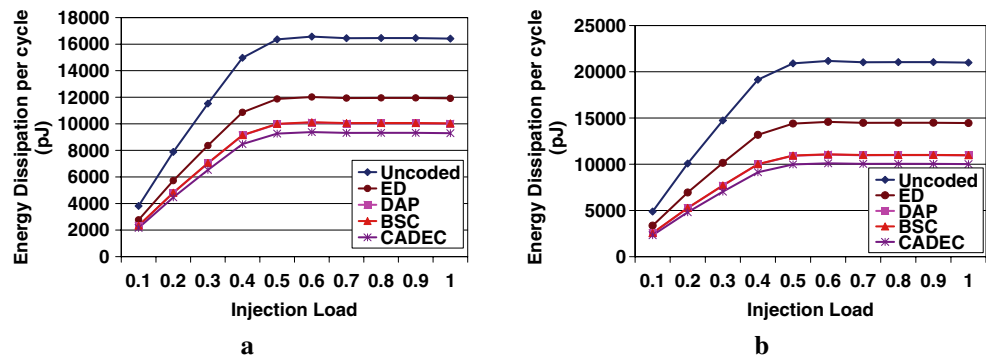
From the above analysis, it is evident that in the event of an error the ED scheme on an average dissipates about two times more energy than the CADEC scheme per bit, ignoring the  $\varepsilon$  term which is much less than unity.

An important point worth mentioning here is that  $E_{bit,DAP} > E_{bit,CADEC}$  and  $E_{bit,ED} > E_{bit,CADEC}$ . This is because the voltage reduction owing to enhancement in reliability is more for the CADEC scheme compared to the other two as seen in Fig. 5. The effective switching capacitance of adjacent wires in presence of crosstalk avoidance coding in CADEC is less than that for the ED scheme which does not guard against crosstalk. Though the coupling capacitances in DAP, BSC and MDR are same as that in CADEC, they need a higher voltage level due to their lower error correction capability. As these two factors, namely, voltage swing and switching capacitance, are the primary contributing factors towards energy dissipation, the energy expenditure per bit per hop is much less for CADEC compared to the other schemes.

**Fig. 7** Average energy dissipation per simulation cycle for all the schemes for MESH-based NoC at **a**  $\lambda=1$  and **b**  $\lambda=4$  with Poisson injection process



**Fig. 8** Average energy dissipation per simulation cycle for all the schemes for FOLDED TORUS-based NoC at **a**  $\lambda=1$  and **b**  $\lambda=4$  with Poisson injection process



**7 Experimental Results and Analysis**

In order to quantify the effectiveness of the proposed CADEC coding scheme on the energy dissipation characteristics of NoC communication infrastructures, we considered a system consisting of 64 IP blocks and mapped them onto MESH, Folded Torus and Butterfly–Fat–Tree (BFT) based NoC architectures as shown in Fig. 6. We assume the NoC to be spread over a die size of 20 mm×20 mm. We compared the performance of the CADEC scheme with the already proposed joint CAC/SEC schemes like DAP, BSC and MDR. We have already shown that the energy dissipation characteristics of DAP and MDR are very similar [17]. Hence, we consider only DAP along with BSC in our comparative analysis. Additionally performance of the CADEC scheme is also compared with the ED-retransmission mechanism. In the simulations, messages were injected with Poisson and self-similar distributions [18]. The routing mechanism used in the simulations depends on the particular network architecture adopted. For the Mesh and Folded Torus architectures e-cube (dimension order) routing [6] was used whereas, for the BFT architecture, LCA (Least Common Ancestor) routing methodology was adopted [18]. The energy dissipations are plotted for each of the three NoC architectures mentioned above. The energy dissipation profiles give the energy dissipated by all messages in the NoC per simulation cycle.

The packet length was assumed to be 16 flits. Simulations were performed assuming 130 nm technology node

parameters. The channel BER is assumed to be  $10^{-20}$  [30] in these simulations.

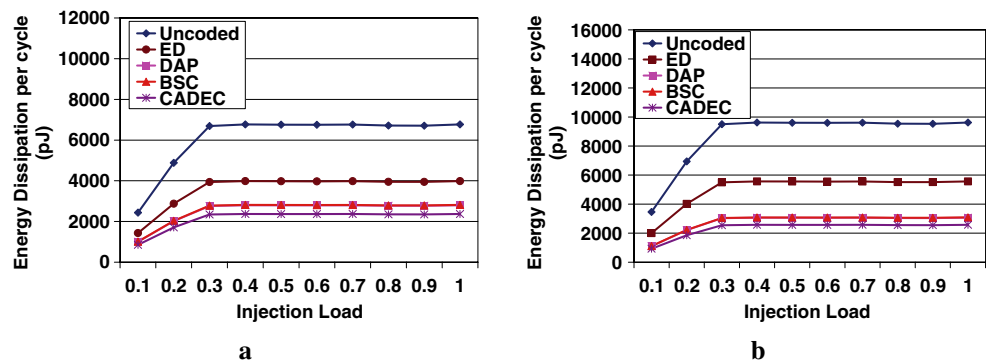
The energy dissipation of each inter-switch wire segment is a function of  $\lambda$ , the ratio of the coupling capacitance to the bulk capacitance. For a given interconnect geometry, the values of  $\lambda$  depend on the metal coverage in upper and lower metal layers. At the 130 nm technology node, the two extreme values of  $\lambda$  are 0.95 and 4.6, respectively [30].

All the schemes have different number of bits in the encoded flit. A fair comparison in terms of energy savings demands that the redundant wires be also taken into account while comparing the energy dissipation profiles. The metric used for comparison thus takes into the account the savings in energy due to the reduced crosstalk, reduced voltage level on the wires, the extra redundant wires, the additional energy dissipated by the codecs, and energy dissipated by the retransmission buffers and ARQ signals for the schemes. An uncoded 32-bit wide flit is considered as the standard for comparison.

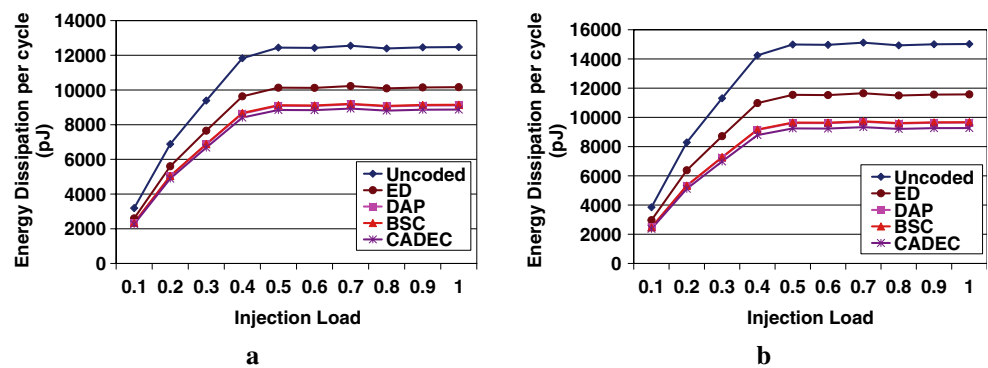
Figures 7a and b show the energy dissipation profile for all the coding schemes (ED, DAP, BSC and CADEC) for  $\lambda=1$  and  $\lambda=4$  respectively, in a Mesh-based NoC architecture.

Figures 8a and b show the energy dissipation profile with  $\lambda=1$  and  $\lambda=4$  respectively for a Folded-Torus based NoC fabric. Figures 9a and b show the energy dissipation profile for a Butterfly–Fat–Tree architecture for the same two extreme cases of  $\lambda$ . In all these experiments the injection process followed the Poisson distribution. The energy expenditure per cycle is least in the case of the CADEC scheme, as it can

**Fig. 9** Average energy dissipation per simulation cycle for all the schemes for BFT-based NoC at **a**  $\lambda=1$  and **b**  $\lambda=4$  with Poisson injection process



**Fig. 10** Average energy dissipation per simulation cycle for all the schemes for MESH-based NoC at **a**  $\lambda=1$  and **b**  $\lambda=4$  with self-similar injection process



reduce the voltage swing more than any of the other schemes due to its double error correcting capability, as discussed in Section 4. In addition to this, the joint CAC and FEC codes (DAP, BSC and CADEC) also reduce the mutual switching capacitances on the inter-switch wire segments, which is another contributing factor in lowering the energy dissipation. The reduction in effective switching capacitance happens only when crosstalk is avoided but not in the ED scheme which does not address crosstalk. Thus the maximum energy dissipation corresponds to the ED scheme.

Figures 10a and b show the energy dissipation profile for a Mesh based NoC by considering a self-similar traffic injection process.

It can be inferred from Figs. 7, 8 and 9 that the reduction in energy dissipation arising out of coding follows the same trend irrespective of the specific NoC, though the absolute value varies from one topology to another. From Fig. 10, it is evident that the energy savings arising as a result of the coding process while considering a self-similar traffic injection is not very different compared to that with Poisson distribution.

## 8 Timing Characteristics

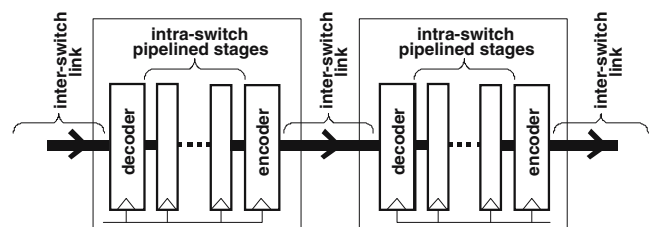
The exchange of data among the constituent blocks in a SoC is becoming an increasingly difficult task because of growing system size and nonscalable global wire delay. To cope with these issues, designers must divide the end-to-end communication medium into multiple pipelined stages, with the delay in each stage comparable to the clock-cycle budget. In NoC architectures, the inter-switch wire segments, along with the switch blocks, constitute a highly pipelined communication medium characterized by link pipelining, deeply pipelined switches, and latency-insensitive component design [3]. The switches generally consist of multiple pipelined stages as shown in Fig. 11. The number of intraswitch pipelined stages can vary with the design style and the features incorporated within the switch blocks. The encoders and decoders are part of intra-switch pipelined stages. In accordance with ITRS [10], a generally accepted

rule of thumb is that the clock cycle of high performance SoCs will saturate at a value in the range of 15 FO4 (Fan-out of 4) delay units. If the delay of the encoder and the decoder and that of the inter-switch wire segments can be constrained within this clock cycle limit then the pipelined communication infrastructure will be maintained.

### 8.1 Inter-Switch Wire Delay

Due to crosstalk with adjacent wires the delay of data propagation through an interconnect increases. This Crosstalk Induced Bus Delay (CIBD) is a function of the worst case crosstalk capacitance between the adjacent wires and it depends on the correlation between transmitted signals. More correlated signals incur less propagation delay compared to completely uncorrelated signals. For an uncoded interconnect the data patterns are generally uncorrelated and consequently it is possible to have the worst case switching scenario, where a data pattern can have a 101 to 010 transition or vice versa. Due to opposite transitions in neighbors on both sides of the victim wire the coupling capacitance of the victim increases by twice for each neighbor and hence it becomes  $(1+4\lambda)C_L$  [25] where  $C_L$  is the load capacitance of the wire including self-capacitance and  $\lambda$  is the ratio of the coupling capacitance to the bulk capacitance as discussed in Section 7. The CIBD for such a situation becomes  $(1+4\lambda)\tau_0$ , where,  $\tau_0$  is the delay of a single individual wire without any coupling.

When error control coding is employed, the correlation between the transmitted data depends on the particular error control code used. For the ED scheme which is implemented using a Hamming code there are no inherent



**Fig. 11** Pipeline data transfer in a NoC considering channel coding

**Table 1** Inter-switch wire delay

Coding scheme	Architecture	Delay (F04)
Uncoded/ED	MESH	0.5
	Folded Torus	2.1
	BFT_3_2 <sup>a</sup>	6.5
	BFT_2_1 <sup>b</sup>	1.6
DAP/BSC/MDR/CADEC	MESH	0.3
	Folded Torus	1.1
	BFT_3_2 <sup>a</sup>	3.5
	BFT_2_1 <sup>b</sup>	0.9

<sup>a</sup> Inter-switch wire spanning levels 2 and 3

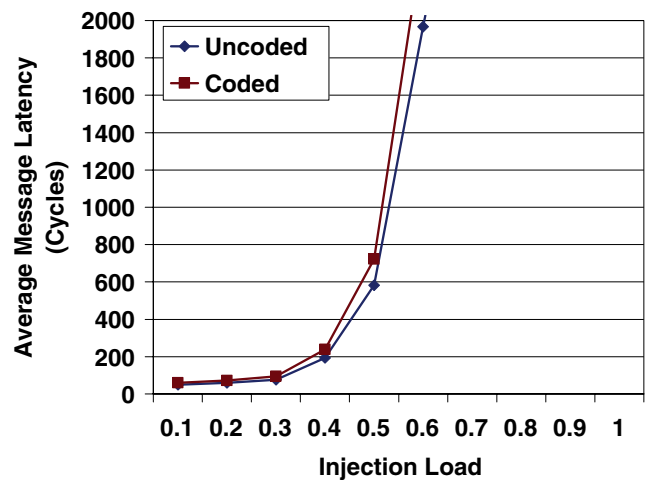
<sup>b</sup> Inter-switch wire spanning levels 2 and 3

crosstalk avoidance characteristics and hence in general the coded data is uncorrelated. Consequently the worst case transition of two neighbors transitioning in opposite directions cannot be avoided and hence the CIBD for the ED scheme is  $(1+4\lambda)\tau_0$ .

For the DAP, BSC, MDR and CADEC schemes the individual bits are all duplicated and hence a 101 or 010 pattern can never occur at all in any code word. This enhances the correlation between transmitted signals. As a result the worst case coupling in the case of such coding schemes reduces to  $(1+2\lambda)C_L$ . This happens because, when neighboring bits switch in the opposite direction, the duplication mechanism forces adjacent pairs of bits on either side of the transition to switch in the same direction. For example, 0011→1100 is the worst transition possible since the bits on the two edges are copies. The worst case CIBD thus becomes  $(1+2\lambda)\tau_0$ . Table 1 shows the delays incurred by the flits while traversing the inter-switch wire segments. It should be noted that for MESH and Folded Torus architectures all the inter-switch wire lengths are the same and hence their delays are equal. On the contrary, in the BFT architecture the wire lengths vary with the level of the tree. As a result the wire delays also vary with the level. For a 64-IP system the BFT-based NoC will have 3 ( $\log_4 64$ ) levels. As shown in Table 1, for all the schemes the inter-switch delays are within the one clock cycle limit of 15F04. Consequently the flits can be transmitted between neighboring switches within a single clock cycle

**Table 2** Critical path delay for each coding scheme

Coding scheme	Codec delay (FO4)	
	Encoder	Decoder
ED	8.2	10.4
DAP	5.8	9.5
BSC	6.0	10.0
MDR	5.8	9.5
CADEC	10.5	10.9



**Fig. 12** Variation of average message latency with injection load

maintaining the pipelined communication architecture of the NoC. As the transmitted signals for DAP, BSC, MDR and CADEC are more correlated than those for Uncoded and ED schemes, they incur less delay in inter-switch wire traversal. Another point worth noting is that as DAP, BSC, MDR and CADEC reduce the wire capacitance by the same amount they incur identical inter-switch delays.

### 8.2 Codec Delay

Through RTL design and synthesis using Synopsys synthesis tools, we obtain the delays along the critical paths of each encoder and decoder for all the coding schemes. The delay values corresponding to all the coding schemes are shown in Table 2. It is evident that all the coding schemes achieve the target delay values within the limit of one clock cycle. As all the individual encoding and decoding operations can be performed within one clock cycle the overall system latency will be the same for all the cases. Thus none of the coding schemes has any advantage over the others in terms of system latency. But the message latency in presence of coding will be more compared to the uncoded situation. Fig. 12 shows the effect of the coding schemes on message latency for the MESH network, with Poisson injection process.

**Table 3** Area overhead of the coding schemes

Coding scheme	Area (2-input NAND gate)
ED	816
DAP	678
BSC	842
MDR	684
CADEC	1357

For all the other NoCs considered here the coding schemes will have similar effect on system latency. Here, the average latency per simulation cycle due to all the messages present in the NoC is considered. As can be seen, the overall message latency in presence of coding increases, but considering the gain in energy savings, the latency overhead is modest.

## 9 Area Overhead

For the sake of complete comparison, we also report the silicon area required by the codec blocks for each of the coding schemes. Through RTL level design and synthesis in Synopsys™ Design Analyzer the silicon area consumed by each codec was obtained as shown in Table 3. The area figures are expressed in units of a minimum sized 2-input NAND gate.

The switches along with the Network Interface (NI) consist of approximately 30K minimum sized NAND gates. Consequently, the area overhead due to each of the coding schemes is not significant. This overhead is a small price to pay for the enhanced reliability and high gains in energy savings from incorporating the coding schemes. Another extra area arises from the retransmission buffers. Following [16], for full throughput operation these buffers account for around 1200 two-input NAND gates per switch port. This additional area overhead can be avoided by adopting a coding scheme with higher error correction capability. As shown in (14), the word error probability and hence the probability of retransmission is proportional to  $\epsilon^3$  for the CADEC scheme. Assuming a typical bit error rate,  $\epsilon$ , of  $10^{-20}$  [30], the probability of retransmission is extremely low. Consequently, even without provision of retransmission the probability of data loss will be negligible. This suggests that higher order error correcting codes will be more area efficient than retransmission-based mechanisms.

## 10 Conclusion

The communication requirements of large multiprocessor SoCs (MP-SoCs) can be conveniently met by the Network on Chip (NoC) paradigm. By incorporating joint crosstalk avoidance and double error correction coding, it is possible to simultaneously enhance the reliability of the NoCs and lower the energy dissipation, despite the associated redundant wires and codec logic requirements. As verified through detailed analysis and simulations, the proposed CADEC scheme lowers the energy dissipation compared to all other existing schemes studied here. The energy savings arise from two factors, namely, the possibility of lowered voltage swing, and reduction of mutual switching capacitance of the inter-switch wire segments. From the analysis carried out in this work, it can

also be concluded that coding schemes with higher order correction capability outperform sole retransmission-based mechanisms in terms of energy and area overhead.

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