

Partha Pratim Pande

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Education

Ph.D. (Electrical & Computer Engineering), University of British Columbia, 2005

M.S (Computer Science), National University of Singapore, 2002

Appointments

Asst. Professor, School of EECS	<i>Washington State University</i>	2005-present
Research Asst	<i>University of British Columbia</i>	2001-2005
Research Scholar	<i>National Univ. of Singapore</i>	2000-2001

Active Research Grants

- CAREER: Reliable On-Chip Wireless Communication Network for Multi-Core Systems. NSF, \$450k, 07/01/09 - 06/30/14.
- DC: Small: Efficient Algorithms for Data-intensive Biocomputing. NSF, 06/01/09 - 05/31/12, \$435k. Anantharaman Kalyanaraman (PI), Partha Pande (Co-PI).

Current Research Interests: My current research principally revolves around the broad topic of Network on Chip (NoC), which has emerged as the communication backbone for multi-core chips. With my graduate students and collaborators I am working on the following projects.

- **On-chip wireless communication network:** Recent research has established characteristics of silicon integrated antennas for intra- and inter-chip communication. Moreover excellent emission and absorption characteristics leading to antenna like behavior in carbon nanotubes (CNTs) are observed recently. In this project we are working on the design methods for wireless NoCs with different types of on-chip antennas.
- **Reliable and Low Power NoC:** We have designed a family of joint crosstalk avoidance and multiple error correction codes (CAC/MEC) and demonstrated how a low power and reliable NoC can be designed by incorporating these CAC/MEC codes.
- **Three dimensional (3D) NoC:** NoC has emerged as the communication backbone for the multi-core chips. The performance improvement arising from the architectural advantages of NoCs will be significantly enhanced if 3D ICs are adopted as the basic fabrication methodology. The amalgamation of two emerging paradigms, NoC and 3D IC, allows for the creation of new structures that enable significant performance enhancements over more traditional solutions. In this project we are investigating characteristics of 3D NoCs.
- **NoC-based hardware accelerators for Biocomputing:** The gap between data generation and data processing is rapidly widening in biocomputing applications, and to close this gap it is imperative to assimilate the latest of breakthroughs in the Integrated Circuit (IC) design community into mainstream biocomputing research. Integrating huge number of processing cores on a single chip can help realize orders of magnitude improvement in performance and eventually will bridge the gap between data generation and data processing. In this project our aim is to design NoC-based hardware accelerators for different biocomputing applications, like sequence alignment and phylogenetic tree construction

Publications:

(1) Journal Papers:

(a) Published/ Accepted

1. Amlan Ganguly, Kevin Chang, Sujay Deb, Partha Pande, Benjamin Belzer, Christof Teuscher, "**Scalable Hybrid Wireless Network-on-Chip Architectures for Multi-Core Systems**", Accepted in IEEE Transactions on Computers (June 2010).
2. Souradip Sarkar, Gaurav Ramesh Kulkarni, Partha Pratim Pande and Ananth Kalyanaraman, "**Network-on-Chip Hardware Accelerators for Biological Sequence Alignment**", IEEE Transactions on Computers, Vol. 59, Issue 1, January 2010, pp. 29-41.
3. Amlan Ganguly, Partha Pratim Pande, Benjamin Belzer, "**Crosstalk-Aware Channel Coding Schemes for Energy Efficient and Reliable NoC Interconnects**", IEEE Transactions on VLSI, Vol. 17, Issue 11, November 2009, pp. 1626-1639.
4. Brett S. Feero, Partha Pratim Pande, "**Networks-On-Chip in a Three Dimensional Environment: A Performance Evaluation**", IEEE Transactions on Computers, vol.58, no. 1, January 2009, pp. 32-45.
5. Amlan Ganguly, Partha Pratim Pande, Benjamin Belzer, Cristian Grecu, "**Design of Low power & Reliable Networks on Chip through joint Crosstalk Avoidance and Multiple Error Correction Coding**", Journal of Electronic Testing: Theory and Applications (JETTA), Special Issue on Defect and Fault Tolerance, June 2008, pp. 67-81.
6. Partha Pratim Pande, Amlan Ganguly, Haibo Zhu, Cristian Grecu, "**Energy Reduction through Crosstalk Avoidance Coding in Networks on Chip**", Journal of System Architecture (JSA), Vol. 54/ 3-4, March-April 2008, pp.441-451.
7. Cristian Grecu, André Ivanov, Res Saleh, Partha Pratim Pande "**Testing Network on Chip Communication Fabrics**", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 26, No. 12, December 2007, pp. 2201-2214.
8. Resve Saleh, Steve Wilton, Shahriar Mirabbasi, Alan Hu, Mark Greenstreet, Guy Lemieux, Partha Pratim Pande, Cristian Grecu, André Ivanov "**System-on-Chip: Reuse and Integration**", Proceedings of IEEE, Volume 94, issue 6, June 2006 pp. 1050-1069.
9. Partha Pratim Pande, Cristian Grecu, André Ivanov, Res Saleh, Giovanni De Micheli "**Design, Synthesis and Test of Networks on Chip: Challenges and Solutions** ", IEEE Design and Test of Computers, Volume 22, Issue 5, Sept.-Oct. 2005 pp. 404 – 413.
10. Cristian Grecu, Partha Pratim Pande, André Ivanov, Res Saleh, "**Timing Analysis of Network on Chip Architectures for MP-SoC Platforms**", Microelectronics Journal, Elsevier, Vol. 36, issue 9, pp. 833-845, August 2005.
11. Partha Pratim Pande, Cristian Grecu, Michael Jones, André Ivanov, Res Saleh, "**Performance Evaluation and Design Trade-offs for Network on Chip Interconnect Architectures**", IEEE Transactions on Computers, vol. 54, no. 8, pp. 1025-1040, August 2005.

(b) Under Review

12. Cristian Grecu, Dipanjan Sengupta, Partha Pande, Andre Ivanov and Res Saleh, “**Self-Repairable SoC Communication Links using Crosspoint Redundancy**”, IEEE Transactions on Computers, under review, (submitted April 2010).

(2) Book Chapter:

13. Partha Pratim Pande, Cristian Grecu, Amlan Ganguly, Andre Ivanov, and Resve Saleh, “**Test and Fault Tolerance of NoC Infrastructures**”, In *Networks-on-Chips: Theory and Practice*, Fayez Gebali, Haytham Elmiligi, and M.Watheq El-Kharashi (eds.), Taylor & Francis Group LLC - CRC Press.
14. Brett Feero and Partha Pratim Pande, “**Three-Dimensional Networks-on-Chip: Performance Evaluation**”, Submitted to “*3D-Architectures and Networks-on-Chip*”, Abbas Shebanyrad, Frédéric Pétrot, and Axel Jantsch (eds.), Morgan Kaufmann

(3) Conference Papers:

(a) Published/Accepted

15. Turbo Majumder, Souradip Sarkar, Partha Pratim Pande and Ananth Kalyanaraman, “**An Optimized NoC Architecture for Accelerating TSP Kernels in Breakpoint Median Problem**”, Proceedings of IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP 2010), 7th – 9th July 2010.
16. Sujay Deb, Amlan Ganguly, Kevin Chang, Partha Pratim Pande, Benjamin Belzer and Deuk Heo, “**Enhancing Performance of Network-on-Chip Architectures with Millimeter-Wave Wireless Interconnects**”, Proceedings of IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP 2010), 7th -9th July, 2010
17. Souradip Sarkar, Turbo Majumder, Ananth Kalyanaraman, Partha Pratim Pande, “**Hardware Accelerators for Biocomputing: A Survey**”, Proceedings of IEEE International Symposium on Circuits and Systems, ISCAS 2010, 30th May – 2nd June, 2010.
18. Partha Pratim Pande, Amlan Ganguly, Kevin Chang, Christof Teuscher, “**Hybrid Wireless Network-on-Chip: A New Paradigm in Multi-Core Design**”, Proceedings of International Workshop on Network-on-Chip Architectures (NoCArc), December 12, 2009.
19. Luca P. Carloni, **Partha Pande** and Yuan Xie, “**Networks-on-Chip in Emerging Interconnect Paradigms: Advantages and Challenges**”, Proceedings of the IEEE International Symposium on Networks-On-Chip, 10-13 May 2009.
20. Amlan Ganguly, Kevin Chang, Partha Pratim Pande, Benjamin Belzer and Alireza Nojeh, “**Performance Evaluation of Wireless Networks on Chip Architectures**”, Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED), 16th-18th March 2009.
21. Cristian Grecu, Andre Ivanov, Resve Saleh, Claudia Rusu, Lorena Anghel, Partha Pratim Pande, Vasile Nuca, “**A flexible network-on-chip simulator for early design space exploration**”, Proceedings of IEEE Microsystems and Nanoelectronics Research Conference, MNRC, October 2008.

22. Alireza Nojeh, Partha Pratim Pande, Amlan Ganguly, Samad Sheikhaei, Benjamin Belzer and Andre Ivanov, "**Reliability of wireless on-chip interconnects based on carbon nanotube antennas**", Proceedings of IEEE International Mixed-Signals, Sensors, and Systems Test Workshop (IMS3TW) June 2008.
23. Partha Pratim Pande, Amlan Ganguly, Benjamin Belzer, Alireza Nojeh, Andre Ivanov, "**Novel Interconnect Infrastructures for Massive Multicore Chips – An Overview**", Proceedings of IEEE International Symposium on Circuits and Systems, ISCAS 2008, 18th-21st May, 2008.
24. Jabulani Nyathi, Souradip Sarkar, Partha Pratim Pande, "**Multiple Clock Domain Synchronization for Network on Chip Architectures**", Proceedings of IEEE International SoC Conference, SOCC 2007, 26th-29th September 2007.
25. Haibo Zhu, Partha Pratim Pande, Cristian Grecu, "**Performance Evaluation of Adaptive Routing Algorithms for achieving Fault Tolerance in NoC Fabrics**", Proceedings of 18th IEEE International Conference on Application-specific Systems, Architectures and Processors, ASAP 2007, July 9th - 11th, 2007.
26. Cristian Grecu, Lorena Anghel, Partha Pratim Pande, André Ivanov, Res Saleh, "**Essential Fault-Tolerance Metrics for NoC Infrastructures**", Proceedings of IEEE International Online Testing Symposium (IOLTS), 9th-11th July, 2007.
27. Partha Pratim Pande, Amlan Ganguly, Brett Feero, Cristian Grecu, "**Applicability of Energy Efficient Coding Methodology to address Signal Integrity in 3D NoC Fabrics**", Proceedings of IEEE International Online Testing Symposium (IOLTS), 9th-11th July, 2007.
28. Amlan Ganguly, Partha Pratim Pande, Benjamin Belzer, Cristian Grecu, "**Addressing Signal Integrity in Networks on Chip Interconnects through Crosstalk-Aware Double Error Correction Coding**", Proceedings of IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 9th-11th May 2007.
29. Brett Feero, Partha Pratim Pande, "**Performance Evaluation for Three-Dimensional Networks-on-Chip**", Proceedings of IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 9th-11th May 2007.
30. Cristian Grecu, André Ivanov, Partha Pande, Axel Jantsch, Erno Salminen, Ümit Y. Ogras, Radu Marculescu, "**Towards Open Network-on-Chip Benchmarks**", Proceedings of IEEE International Symposium on Networks-on-Chip (NOCS' 07), 7-9 May 2007.
31. Cristian Grecu, André Ivanov, Res Saleh, Partha Pratim Pande, "**NoC Interconnect Yield Improvement Using Crosspoint Redundancy**", Proceedings of 21st IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT'06), 2nd-4th October 2006.
32. Partha Pratim Pande, Amlan Ganguly, Brett Feero, Benjamin Belzer, Cristian Grecu, "**Design of Low Power and Reliable Networks on Chip through joint crosstalk avoidance and forward error correction coding**", Proceedings of 21st IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT'06), 2nd-4th October 2006.

33. Partha Pratim Pande, Haibo Zhu, Amlan Ganguly, Cristian Grecu, "**Crosstalk-aware Energy Reduction in NoC Communication Fabrics**", Proceedings of IEEE International SOC Conference, SOCC 2006, 24th-27th September, 2006.
34. Partha Pratim Pande, Haibo Zhu, Amlan Ganguly, Cristian Grecu, "**Energy Reduction through Crosstalk Avoidance Coding in NoC Paradigm**", Proceedings of 9th Euromicro Conference on Digital System Design, DSD 2006, 30th August-1st September 2006.
35. Cristian Grecu, André Ivanov, Res Saleh, Egor S. Sogomonyan, Partha Pratim Pande, "**On-line Fault Detection and Location for NoC Interconnects**", Proceedings of 12th IEEE International On-Line Testing Symposium, IOLTS 2006, July 10-12 2006.
36. Cristian Grecu, Partha Pratim Pande, André Ivanov, Res Saleh, "**BIST for Network on Chip Interconnect Infrastructures**", Proceedings of 24th IEEE VLSI Test Symposium, VTS 2006, 30th April – 4th May, 2006.
37. Cristian Grecu, Partha Pratim Pande, Baosheng Wang, André Ivanov, Res Saleh, "**Methodologies and Algorithms for Testing Switch-Based NoC Interconnects**", Proceedings of IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT 2005), 3-5th October, 2005, Monterey, USA.
38. Partha Pratim Pande, Cristian Grecu, Michael Jones, André Ivanov, Res Saleh, "**Effect of traffic localization on energy dissipation in NoC-based interconnect infrastructures**", Proceedings of IEEE International Symposium on Circuits and Systems, ISCAS 2005, 23-26th May, Kobe Japan.
39. Partha Pratim Pande, Cristian Grecu, Michael Jones, André Ivanov, Res Saleh, "**Evaluation of MP-SoC Interconnect Architectures: A Case Study**", Proceedings of 4th IWSOC, 19th-21st July, 2004, Banff, Alberta, Canada.
40. Cristian Grecu, Partha Pratim Pande, André Ivanov, Res Saleh "**Structured Interconnect Architecture: A Solution for the Non-Scalability of Bus-Based SoCs**", Proceedings of GLSVLSI 2004, 26-28th April, Boston.
41. Cristian Grecu, Partha Pratim Pande, André Ivanov, Res Saleh, "**A Scalable Communication-Centric SoC Interconnect Architecture**", Proceedings of IEEE International Symposium on Quality Electronic Design, ISQED 2004, San Jose, California, USA, 22-24 March, 2004.
42. Partha Pratim Pande, Cristian Grecu, André Ivanov, Res Saleh, "**Switch-Based Interconnect Architecture for Future Systems on Chip**", Proceedings of SPIE, VLSI Circuits and Systems, 2003, Maspalomas, Gran Canaria, Spain.
43. Partha Pratim Pande, Cristian Grecu, André Ivanov, Res Saleh, "**High-Throughput Switch-Based Interconnect for Future SoCs**", Proceedings of IEEE International Workshop on SoC for Real Time Applications, 2003, Calgary, Canada.
44. Partha Pratim Pande, Cristian Grecu, André Ivanov, Res Saleh, "**Design of a Switch for Network on Chip Applications**", Proceedings of IEEE International Symposium on Circuits and Systems, ISCAS 2003, Bangkok, Thailand.

Synergistic Activities:

- (1) Associate Editor, IEEE Design and Test of computers
- (2) Guest Editor, IEEE Design and Test of Computers, Special Issue on Emerging Interconnect Technologies for Gigascale Integration.
- (3) Program Committee member of the following conferences
 - IEEE International Midwest Symposium on Circuits and Systems, MWSCAS, 2007 (Co-chair for the Test and Characterization track)
 - IEEE International Midwest Symposium on Circuits and Systems, MWSCAS, 2010, Publication Chair.
 - IEEE International online testing symposium, IOLTS (2007-2010)
 - Asian Test Symposium, ATS (2007, 2008)
 - IEEE International Workshop on Electronic Design, Test and Applications, DELTA (2008-2010)
 - IEEE International Symposium on Networks-on-Chip (NOCS 2009, 2010)
- (4) Organizer of the Hot Topic session “*Fault Tolerant Nanoscale Architectures – the Challenges and Emerging Solutions*” 25th IEEE VLSI Test Symposium, VTS 07
- (5) Presenter in the Hot Topic Session, “*Signal Integrity: How Can it be Designed into Multiprocessor Platforms, Systems on-Chip, and Systems in-Package?*” 24th IEEE VLSI Test Symposium, VTS 06
- (6) Special session organizer and session chair, IEEE International Symposium on Circuits and Systems, ISCAS 2008, 2010.
- (7) Special session organizer, IEEE International Green computing Conference.
- (8) Member, Computer Engineering Curriculum Committee, School of EECS, Washington State University
- (9) Member, Scholarship Committee, School of EECS, Washington State University
- (10) Reviewer for conferences like Design Automation & Test in Europe (DATE), International Conference on Computer Aided Design (ICCAD), Design Automation Conference (DAC), VLSI Test Symposium (VTS), International Test Conference (ITC), International Symposium on Circuits and Systems (ISCAS) and journals like IEEE Transaction on VLSI, IEEE Design and Test, IEEE Transactions on computer-aided design of Integrated Circuits and Systems.

Graduate Students Supervision:

- (a) Current Graduate Students:
 - Amlan Ganguly (PhD, expected graduation, August, 2010)
 - Souradip Sarkar (PhD, expected graduation, December 2010)
 - Sujay Deb (PhD, expected graduation, December 2011)
 - Kevin Chang (PhD, expected graduation, December 2011)

- Turbo Majumder (PhD, expected graduation, December 2012)
- Steve Hung (MS, expected graduation, May 2011)
- Miralem Cosic (MS, expected graduation, May 2011)
- Divya Krishnan (MS (non-thesis), expected graduation, July 2010)
- Paul Wettin (PhD, starting August 2010)
- Jacob Murray (PhD, starting August 2010)

(b) Graduated:

- Amlan Ganguly (MS, May 2007, currently pursuing PhD at WSU)
- Haibo Zhu (MS, July 2007, currently employed at LINK_A Media Devices, San Jose, USA)
- Souradip Sarkar (MS, December 2007, currently pursuing PhD at WSU)
- Brett Feero (MS, May 2008, currently employed at ARM ltd, Cambridge, UK)
- Kevin Chang (MS, December 2008, currently pursuing PhD at WSU)

Committee Member:

- Syryanarayana Tatapudi (PhD, Graduated, May 2006)
- Daniel R. Blum (PhD, Graduated, May 2007)
- Ray Robert Rydberg III (PhD, Graduated, May 2009)
- Billy J Hamon (MS, Graduated, December 2008)
- Nancy Shah (MS, Graduated, January 2009)
- Jeremy Asmussen (MS, Graduated, December 2009)
- Alex O. Mikul (MS, Graduated, December 2009)
- Gaurav Ramesh Kulkarni (MS, December 2009)

Teaching Evaluation:

Course Number	Semester	Evaluation (5)
EE434	Fall 2005	4.51
EE582	Spring 2006	4.29
EE434	Fall 2006	4.77
EE434	Fall 2007	4.49
EE587	Spring 2008	4.39
EE434	Fall 2008	4.19
EE334	Spring 2009	4.02
EE587	Spring 2009	4.56
EE434	Fall 2009	4.05
EE586	Fall 2009	4.25
EE587	Spring 2010	4.56

Invited Presentations:

1. Intel Circuit Research Lab, 16th January, 2009, Hillsboro, Portland.
2. IEEE Solid-State Circuits Society, Vancouver Chapter, April 2008
3. 11th IEEE VLSI Design and Test Symposium (VDAT), August, 2007, Kolkata, India.
4. G. S. Sanyal School of Telecommunications, Indian Institute of Technology (IIT), Kharagpur, India, August 2007.
5. Institute of Radio Physics & Electronics, Calcutta University, India, July 2007.