

Range-enabled CCAMs for Packet Classifiers

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Abstract—Packet classification is a fundamental task for network devices such as edge routers, firewalls, and intrusion detection systems. Currently, most vendors use Ternary Content Addressable Memories (TCAMs) to achieve high-performance packet classification. TCAMs use parallel hardware to check all rules simultaneously. Despite their high speed, TCAMs have a fundamental in dealing with ranges efficiently. Many packet classification rules contain range specifications, each of which needs to be translated into multiple prefixes to store in TCAMs. Such translation may result in an explosive increase in the number of required TCAM entries. So the rule sets are usually compressed before stored in TCAM entries, but this kind of compressions make the rule set update very complex and degrade the overall performance. In this paper, we propose Comparator Content Addressable Memories (CCAMs), which can store ranges in CCAM entries besides ternary state numbers. In our algorithm, the hardware can be configured to store all kinds of Port number ranges. If a rule contains any two-direction ranges, only two CCAM entries are needed to store it, otherwise, each rule can be stored in a single CCAM entry. Our simulations show that CCAMs consumes about 27.6% entries compared with original TCAMs. Considering the transistor consumption, our approach saved about 66.4% transistors. Furthermore, the update process of CCAMs can be as fast as TCAMs usage without any compressions.

I. INTRODUCTION

II. RELATED WORK

III. CHALLENGES OF TCAMs USED IN PACKET CLASSIFIERS

A. Range Explosion

IV. SIMULATION RESULTS

[1]–[6].

V. CONCLUSION

In this paper, we propose Comparator Content Addressable Memories (CCAMs) to solve range explosion and slow rule set update problems. Our algorithm can store ranges in CCAM entries besides ternary state numbers. In our algorithm, the hardware can be configured to store all kinds of Port number ranges. If a rule contains any two-direction ranges, only two CCAM entries are needed to store it, otherwise, each rule can be stored in a single CCAM entry. Our simulations show that CCAMs consumes about 27.6% entries compared with original TCAMs. Considering the transistor consumption, our approach saved about 66.4% transistors. Furthermore, the update process of CCAMs can be as fast as TCAMs usage without any compressions and pipeline is used to increase the throughput.

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