Description

Question 1: Describe the following VHDL modeling constructs: Entity Declaration, behavioral architectural body, structural architecture body, process statement, signal assignment statement and port map.

Question 2: Write a counter model with a clock input “clk” of type “bit”, and an output “q” of type integer. The behavioral architecture body should contain a process that declares a count variable initialized to zero. The process should wait for changes on “clk”. When “clk” changes to “1”, the process should increment the count and assign its value to the output port.

Question 3: Write an if statement that sets a variable “odd” to “1” if an integer “n” is odd and “0” if it is even.

Question 4: Write a model for a counter with an output port of type “natural”, initially set to 15. When the “clk” input changes to “1”, the counter decrements by one. After counting down to zero, the counter wraps back to 15 on the next clock edge.

What to Turn in for This Assignment

For this assignment, you must turn in the following items:

Answers to the above questions. It MUST be typed. No handwritten answers accepted.

How Your Assignment will be Evaluated

Your document will be evaluated on the completeness. This assignment is worth 60 points.