Midterm Exam #1 Study Guide

The exam will cover Chapters 2 through 6 of the text.

The following sections of Chapter 2 are not covered:
   2.1, 2.2, 2.10, 2.11, 2.12, 2.13

All sections of Chapter 3 and 4 are covered. However, only the assembler directives and instructions noted below are covered.

The following information in chapter 5 is not covered:
   Section 5.6 – No questions will be asked about the interrupt system hardware external to the CPU.

In Chapter 6, the following sections are not covered:
   6.7, 6.9, 6.11, 6.12

In addition to the material from the text book, be familiar with the C language control constructs and the use of stack frames for accessing parameters and local variables within procedures.

You are expected to know the following assembler directives and operators:
   SEGMENT
   ENDS
   END
   PROC
   ENDP
   ASSUME
   DB
   DW
   DD
   SEG
   OFFSET
   BYTE PTR
   WORD PTR
   DWORD PTR
   DUP

You should be familiar with the operation of the following instructions and the affect that they may have on the Flags:
   **Data Transfer:** MOV (all forms), PUSH, POP, PUSHF, POPF, LEA, LDS/LES
   **String Instructions:** MOV, LODS, STOS, CMPS, SCAS (with or without REP prefix).
   **Arithmetic and Logical:** ADD, ADC, SUB, SBB, CMP, NEG, INC, DEC, DAA, AAA, NOT, AND, OR, XOR, TEST

   **Bit Manipulation:** SHL/SAL, SHR, SAR, ROL, RCL, ROR, RCR
**Program Transfer:** JMP, Jcc (conditional jumps), LOOP, JCXZ, CALL, RET, INT, IRET

**Processor Control:** CLC, STC, CMC, CLD, STD, CLI, STI, HLT, NOP

**Memory Addressing:**
- Know all memory addressing modes.
- Know what the term *effective address* means, and how the CPU calculates effective addresses for each addressing mode.
- Know how the CPU calculates physical addresses in memory, and the difference between *effective address*, *physical address*, and the canonical *segment:offset* form of an address.
- Know the Intel convention for the byte order of data in memory. (i.e. the lowest byte of the data is stored at the lowest memory address, the highest byte of the data is stored at the highest memory address). Know how to read a memory display from the debugger.
- Know the order in which data appears on the stack. The stack grows down (i.e. push decrements SP). SP always points to the current top of the stack. (i.e. PUSH decrements SP first and then writes the value to the stack, POP reads the value from the stack and then increments SP).

You do not need to know any 32 bit addressing modes or instructions. There will be no questions on the exam that pertain to any processor other than the 8088/8086.

**FLAGS register:** You need to know the meanings of the various condition code bits in the flags register. You do not need to know the specific bit positions for the flags bits.

**Interrupt System:**
- Know how the CPU determines the address of an Interrupt Service Routine.
- Know what the sequence of operations is when the CPU responds to an interrupt.
- Know the layout of information on the stack during interrupt processing.
- Know which interrupt vectors correspond to which special interrupts. (e.g. the trace interrupt uses the INT 1 vector, NMI uses the INT 2 vector, the breakpoint interrupt uses the INT 3 vector, etc.)

Know how to do simple conversions between HEX, BINARY, and DECIMAL.

There will be at least one problem where you are asked to write a short subroutine that conforms to a given input/output specification.

There will be at least one problem where you are given the contents of memory, the contents of the CPU registers and a listing of a sequence of instructions and are asked to answer questions about the execution of the program based on the given values.