EE 587
SYSTEM ON CHIP DESIGN & TEST
FINAL EXAM
1st May 2012

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Time: 120 minutes
Maximum Points: 50
(1) Consider an n-bit bus. Add one extra line as shown in the figure. When the n-bits of the bus switches from 1 to 0 what will be the dynamic power dissipation? What is the effect of adding an extra line?
(b) If you consider the inductive effects of a line then what is the effect on buffer insertion? Does the number of buffer changes to keep the same delay. What happens to the short circuit current? [2]
(a) Suppose you are designing a datapath using custom-layout techniques. Your data flows from left to right, as shown in the following two diagrams. In the first diagram, the clock is driven by a driver on the left side of the chip, and the clock propagates from left to right. In the second diagram, the clock is driven by a driver on the right side of the chip, and the clock propagates from the right to the left. Which design is safer?

Layout 1:

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CLK -> D Q -> Combinational Logic -> D Q
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Layout 2:

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D Q -> Combinational Logic -> D Q
CLK
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(b) Consider the two clock lines shown in the figure below. Compare the capacitance between the clock lines in the two configurations. Is there any difference between the inductive effects of these two lines? Explain.
(c) What is the role of the EN signal in the following circuit?
Consider an isolated 2mm long and 1μm wide M1 (Metal1) wire over a silicon substrate driven by an inverter that has zero resistance and parasitic output capacitance. How will the wire delay change for the following cases? Explain your reasoning in each case.

a. If the wire width is doubled.
b. If the wire length is halved.
c. If the wire thickness is doubled.
d. If thickness of the oxide between the M1 and the substrate is doubled. [6]
(b) You are asked to design a 4-input NOR gate. Suppose, you have two options, static CMOS & Pseudo NMOS. Which one will dissipate less dynamic power? [2]
(c) Explain how the following circuit can achieve both high speed and low power operation. You just need to explain the principle. Does this configuration have any effect on the noise margin of the circuit?
(4) (a) Consider the following multiplier circuit whose inputs change every cycle but whose output conditionally feeds an ALU. What is the problem with this circuit? Modify this circuit so that its power dissipation is reduced.
(b) What is Weighted Switching Activity (WSA)? In a LFSR-based testing how can you control the test patterns to reduce the WSA? [2]
(c) In the following circuit when Q goes from 1 to 0, then is it possible for the internal nodes of the NMOS tree can have a full swing to logic 1? If not, explain why?
Compute the first eight patterns generated by the modular LFSR with characteristic polynomial $f(x) = x^3 + x + 1$ assuming that the LFSR was initialized to "001" with the 1 in the least significant bit.
(b) What are the values of the control signals B1 and B2, if we want to use the following BILBO in the “pattern generator” mode? Show the path activated in this mode. [2]
(c) In the following circuit the PMOS transistor is stuck-open. Write down the sequence of test vectors to detect this fault. What will be the output of the faulty circuit? [2]
6. (a) Consider the following SoC. You have to test Core A for a possible bridging fault. What test methodology needs to be adopted? What precaution needs to be followed? How can you do this? [3]
(b) How should you modify the following scan flip-flop so that the module under test (MUT) inputs remains unchanged during a shift operation? [2]
(c) What is the total number of single stuck-at faults in the following circuit? Derive the equivalence collapsed set. What is the collapse ratio?
7. (a) In the following two flip-flop-based circuits which one is more power efficient and why? [2]
(b) By trading-off positive timing slack, dynamic power of a data path circuit can be reduced. Will it affect the yield of the chip? Please explain. [2]