Washington State University  
School of EECS  
Electrical Engineering Course Assessment Report

Course Number: EE324  
Course Title: Fundamentals of Digital Systems  
Semester Offered: Fall 2006  
Instructor: Clint Cole  
10th Day Enrollment 23  
Number Completing Successfully (C grade or better) 21

I. Assessment Outcomes from the Course Syllabus

- (A) Ability to apply knowledge of mathematics, science and engineering.  
- (B) Ability to design and conduct experiments as well as analyze and interpret data.  
- (C) Ability to design a system, component, or process to meet desired needs.  
- (D) Ability to function on multidisciplinary teams.  
- (E) Ability to identify, formulate, and solve engineering problems.  
- (G) Ability to communicate effectively in written and oral formats.  
- (H) A broad education necessary to understand the impact of engineering solutions in global, economic, and societal context.  
- (I) Recognize the need for, and have the ability to engage in life long learning.  
- (J) Have a broad education and knowledge of contemporary issues.  
- (K) Ability to use techniques, skills and modern engineering tools necessary for engineering practices.  
- (F) An understanding of professional and ethical responsibility.

II. List of Course Topics from the Course Syllabus

1. Basic memory circuits;  
2. Design of synchronous circuits and state machines using various models;  
3. Inputs and outputs to/from synchronous circuits;  
4. Clock and reset signals;  
5. VHDL and coding methods for synchronous circuits;  
6. FPGA (and other PLD) architectures;  
7. CAD tools and methods;  
8. System-level design topics;  
9. Basic digital system electronics, including power delivery and signal integrity issues.
III. Course Assessment Summary Table: one row of the table should be devoted to each of the checked outcomes in part I.

<table>
<thead>
<tr>
<th>Outcome</th>
<th>Topics</th>
<th>Specific Measures (Samples available for inspection.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(A) Ability to apply knowledge of mathematics, science and engineering.</td>
<td>1-9</td>
<td>Exam 1: problems 1 through 8; Final Exam: problems 1 through 5; Homework/Lab 12, 14, 15, 16, and EC</td>
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<tr>
<td>(B) Ability to design and conduct experiments as well as analyze and interpret data.</td>
<td>2, 3, 7, 8</td>
<td>Homework/Lab 12, 14, 15, 16, and EC</td>
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<tr>
<td>(C) Ability to design a system, component, or process to meet desired needs.</td>
<td>1-9</td>
<td>Homework/Lab 12, 14, 15, 16, and EC</td>
</tr>
<tr>
<td>(E) Ability to identify, formulate, and solve engineering problems.</td>
<td>1-5, 8, 9</td>
<td>Homework/Lab 12, 14, 15, 16, and EC</td>
</tr>
<tr>
<td>(G) Ability to communicate effectively in written and oral formats.</td>
<td>8</td>
<td>Homework/Lab 14, 16</td>
</tr>
<tr>
<td>(K) Ability to use techniques, skills and modern engineering tools necessary for engineering practices.</td>
<td>1-9</td>
<td>Homework/Lab 12, 14, 15, 16, and EC, Exam 1: problems 1 through 8; Final Exam: problems 1 through 5</td>
</tr>
</tbody>
</table>

IV. Using the table as a guide, for each outcome summarize your evaluation of the students' achievement of that outcome; cite student performance on the identified measures as evidence to support your conclusions.

(A) Ability to apply knowledge of mathematics, science and engineering.

The class is structured around the laboratory, where students must regularly complete designs that require mathematical and/or scientific knowledge. All designs also require an increasing fund of engineering knowledge and skill. For example, the second lab project (numbered lab experiment #14) requires that students design a digital circuit to synthesize various waveshapes, and a pulse-width-modulator circuit to output the synthesized wave to a reconstruction filter. To adequately design for sample rate and filter characteristics, students must understand applicable mathematical analysis and modeling, as well as possess the engineering skills to implement the circuit. All four lab projects this semester required in-depth knowledge of engineering methods and technologies. The completion rate for all students across all four lab designs was 96%, and the average score was 88%. The lab assistants understand a large part of their job is to ensure that all students complete their own work, and adequate support is provided to the students to make sure this goal is met.
The examinations in the class probed students grasp of the concepts practiced in the lab. The first three problems (and #8) of exam #1 tested student's understanding of the structural design of sequential circuits, and the remaining problems tested their behavioral design abilities. The relatively high average (76) was a good indicator that students comprehend the material.

(B) Ability to design and conduct experiments as well as analyze and interpret data.
Lab design projects are chosen in part to eliminate the possibility of students finding solutions on the web, or otherwise taking advantage of previously completed work. To arrive at adequate solutions, students must experiment – they must build real circuits, test them and interact with them, and use their increasing knowledge to improve their design. Oscilloscopes, meters, and analyzers are available in the labs, and students use these routinely to gain critical knowledge about their circuits. They also make extensive use of simulators and other CAD tools to probe their designs. Without this build-test-measure-improve design approach, students would not be able to complete the lab designs.

(C) Ability to design a system, component, or process to meet desired needs.
This is probably the strongest aspect of this class – the intent of the class can be adequately summarized as providing students with the knowledge and skills they need to design a system, component, algorithm, or process to meet a stated need. Virtually all lab designs completed by students, and all examples presented in class are geared towards increasing students design skills. The exams also probe students understanding of design methods, requirements, and technologies. In fact, the final exam is centered on a system design problem that requires students to consider all aspects of a given design requirement.

Performance on the lab designs and on the tests, and in particular on the final exam, shows that virtually all of the students comprehended that class materials well, and that even average students gained an acceptable level of design ability.

(E) Ability to identify, formulate and solve engineering problems.
As with C above, the intent of the class is to provide students with the knowledge and skills necessary to solve a wide variety of engineering problems. Every lab assignment required students to design significant circuits to solve real engineering problems. In their solutions, students need to overcome their own personal shortcomings – not all students have equal design abilities when entering the class. In the process of solving more involved problems, students must consistently identify areas where they are weak, and devices ways to solve new problems. This requires them to identify possible design solutions, pursue them to learn whether their approach will work, and from their growing experience base, formulate solutions to problems.

The high lab experiment completion rate (96%), and high average scores (88%) indicate students gained the ability to solve engineering problems, and therefore the ability to identify their own particular problems, and formulate solutions to them.
(K) Ability to use techniques, skills and modern engineering tools necessary for engineering practices.

State-of-the-art CAD tools (Xilinx ISE 8.2, released 8/2006) and technologies (Xilinx Spartan 3E FPGA, released 1/2006) were used in the class, as well as new test and measurement equipment and up-to-date reference and educative materials. Some lab designs required that students find electronic components using web resources, and supplemental design information as well.

Throughout the class, structural and then behavioral designs are required, and the students must use simulators (ModelSim 5.6) and analyzers to verify their designs. Behavioral designs must be synthesized to a particular technology, and then verified against design specifications. In short, the entire skill set used by practicing engineers today is exercised at some point in the class.

V. Qualitative Assessment of Student Performance: using the arguments above and other data support the claim that students who completed this course with a grade of C or better have achieved each of the intended outcomes of this course.

The lab designs gave students a great deal of exposure to modern design methods and technologies. The design requirements in this class are more challenging than those found in similar classes at most other Universities. All students are required to take several designs from initial concept through to implementation and demonstration in hardware, which means each of them must gain proficiency with modern tools and methods. The exams challenged student’s comprehension of the course materials, and gave the course instructor a method to ensure that each student was building an adequate fund of knowledge.

The high completion rate on the lab experiments (96%) and high average score (88%), combined with the adequate averages on the exams (76% and 79%) indicate that students achieved an adequate, and in fact very respectable knowledge and skill base.

On a further note, I personally maintain working relationships with many engineers at some of the nations best engineering companies and engineering universities. I routinely share with my colleagues the nature and scope of the lab designs I assign, and seek their inputs. Through these liaisons, I am confident that the design work in this class is topical, relevant, and instrumental in imparting valuable knowledge and skills.

VI. Concerns: state any concerns you may hold about this class – were the students adequately prepared coming into it? Are there topics or outcomes where (some) students were weak after completing the course? Other concerns? Were there any comments on students’ course evaluations that should be addressed in future instances of the course? This section is very important for improving our program: it provides critical input to the curriculum committee for identifying areas requiring attention.
Students who have attended WSU for prerequisite classes prior to taking this class fair quite well; students transferring from other schools tend to struggle more, at least in the early parts of the class. Because this class uses modern design tools, methods, and technologies, it is essential that students gain a degree of exposure to these tools and methods prior to taking this class. That prior exposure is provided in prerequisite classes here at WSU, but not so much at other institutions. Transfer students have all ultimately been successful, but they must work extra hard at the outset of the class.

A key to keeping this class successful is access to skilled and experienced lab assistants. So far, we have been able to hire very good assistants, and we must make this a priority for future classes as well. There is simply too much material in this class, and the imparted and necessary skills are advanced enough that there is not adequate time to train lab assistants in the early part of the class.

Perhaps one current weakness is that the students should be required to make greater use of test and measurement equipment to verify their designs. We are in the process of acquiring better logic analyzers (we already have and use good oscilloscopes), and we are creating enhanced experiments that require more use of T&M equipment. Once all students use equipment on a more regular basis, this class will contain all necessary ingredients to impart a complete range of relevant skills.

Finally, because of the use of modern CAD software, we must ensure the computing infrastructure keeps pace. New computers will be required in the lab at least every three years. So far, we have been able to provide very good computers in the design lab, and this must continue to be the case.

Signature: Date: 2/23/07