EE 434
ASIC and Digital Systems

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Preliminaries
VLSI Design


<table>
<thead>
<tr>
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<th>Freq</th>
<th>Area</th>
<th>Power</th>
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<tr>
<td>64-bit integer multiplier / 1GHz / 0.1mm² / 0.1mW</td>
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C/C++, Verilog, VHDL, ...

module imul_64 (a, b, clk, out64);
input a, b, clk; output out64; ...
endmodule

Netlist  →  Layout  →  Bare die  →  Chip

Physical Design Automation of VLSI Circuits and Systems
From RTL Code to a Chip

module mul64 (in_1, in_2, clk, out_1);
    input [31:0] in_1, in_2;
    input clk;
    output [63:0] out_1;

    reg [63:0] int_stage1;
    reg [63:0] int_stage2;

    always @ (posedge clk)
        begin
            ...
            end

endmodule
From RTL Code to a Chip

RTL Code (HDL) → Synthesis → Tech library (e.g., 45nm)

Module declaration:
```
module mul64 (in_1, in_2, clk, out_1);
  input [31:0] in_1, in_2;
  input clk;
  output [63:0] out_1;

  reg [63:0] int_stage1;
  reg [63:0] int_stage2;

  always @(posedge clk)
  begin
    ...
  end
endmodule
```

Tech-specific logic gates:
```
module mul64 (in_1, in_2, clk, out_1);
  input [31:0] in_1, in_2;
  input clk;
  output [63:0] out_1;

  NAND2 X1 ( .A(in_1[0]), .B(in_2[0]), .Z(n1) );
  FA X1 ( .A(in_1[0]), .B(in_2[0]), .CI(1'b0), .S(n2), .CO(n3) );
  ...
endmodule
```
From RTL Code to a Chip

RTL Code (HDL) → Synthesis → Physical Design
From RTL Code to a Chip

- RTL Code (HDL)
- Synthesis
- Physical Design
- Fabrication
From RTL Code to a Chip

RTL Code (HDL) → Synthesis → Physical Design → Fabrication → Packaging
## VLSI Design

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<th>Full custom</th>
<th>ASIC</th>
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<tr>
<td>Design</td>
<td>Manual</td>
<td>Automatic</td>
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<tr>
<td>TRs</td>
<td>Manually drawn</td>
<td>Standard-cell based</td>
</tr>
<tr>
<td>Placement &amp; Routing</td>
<td>Custom</td>
<td>Automatic</td>
</tr>
<tr>
<td>Development time</td>
<td>Several months</td>
<td>A few days ~ weeks</td>
</tr>
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</table>
Standard-Cell-Based Design

• Provides
  – good performance
  – low power
  – small area
  – …

• Other design styles
  – FPGA
  – PLA
  – …
Standard-Cell-Based Design

• Standard cells
  – A set of logic gates
  – Have the same height.
  – Width varies.
  – Pre-characterized for timing and power analysis.
Standard Cells (Layout)

INV

NAND2
Standard Cells (Layout)

Top-down view

Side view

Physical Design Automation of VLSI Circuits and Systems
Design Rules

①: Min. distance (poly, contact)
②: Min. distance (metal 1)
③: Min. distance (p-active, n-well boundary)
④: Min. width (poly)
⑤: Min. width (metal 1)
⑥: Min. distance (contact)
⑦: Min. distance (contact, n-well boundary)
Standard Cells (Layout)

- n+ (n-implant)
- p+ (p-implant)
- contact
- poly (gate)
- metal 1
- - - - cell boundary

INV

NAND2
Standard Cells (Abstract)

**INV**

- **in**
- **out**

- **VDD**
- **GND**

**NAND2**

- **in1**
- **in2**
- **out**

- **VDD**
- **GND**

**metals 1**

---

**cell boundary**
Standard-Cell-Based Design

- - - - cell boundary

metal 1

via12

metal 2
Standard-Cell-Based Design

• Deal with
  – Standard cells (pre-drawn and pre-characterized)
  – Routing layers (M1, via12, M2, via23, …)
Standard-Cell-Based Design

• Intellectual Property (IP) blocks
  – Pre-created blocks
    • Memory
    • Arithmetic
    • Cryptographic
    • DSP
    • Controller
    • …
Standard-Cell-Based Design
Delay Calculation & Timing Analysis

- Pre-characterized cells

```plaintext
Input transition (ns)  Output capacitance (fF)

Pre-characterized values

Index_1

Index_2

cell_fall(Timing_7_7) {
    index_1 ("0.00117378,0.00472397,0.0171859,0.0409838,0.0780596,0.130081,0.198535");
    index_2 ("0.365616,1.854900,3.709790,7.419590,14.839200,29.678300,59.356700");
    values ("0.00683090,0.0100142,0.0139116,0.0216539,0.0370876,0.0679222,0.129575", \ 
        "0.00801780,0.0112344,0.0151696,0.0229509,0.0384185,0.0692724,0.130935", \ 
        "0.010663,0.0155786,0.0201499,0.0279195,0.0433427,0.0741885,0.135850", \ 
        "0.0127253,0.0190883,0.0256634,0.0364481,0.0533390,0.0839029,0.145413", \ 
        "0.0128360,0.0209729,0.0293903,0.0433808,0.0656528,0.0997348,0.160709", \ 
        "0.0112031,0.0210972,0.0313125,0.0483362,0.0756855,0.118141,0.182879", \ 
        "0.00772654,0.0192683,0.0312780,0.0512843,0.0834863,0.133996,0.210841");
}
```

Delay (29ps)
Delay Calculation

- Interconnect delay

\[ R = \rho \frac{l}{t \cdot w} \quad C = \epsilon \frac{t \cdot l}{s} \]

\[ \text{Delay} \propto RC \propto l^2 \]
Timing Analysis
Standard-Cell-Based Design

• What should we do?
  – Find the locations of the macros.
  – Find the locations of the standard cells.
  – Route the macros and the standard cells.
    • Power/ground
    • Signal
    • Clock
    • Bus
  – Extract parasitic RC.
  – Analyze the final layout.
    • Timing (clock frequency)
    • Power consumption (dynamic / leakage)
    • Area
    • Power integrity
    • Signal integrity
    • Thermal
Standard-Cell-Based Design

- Floorplanning (macro placement)
- Placement (standard cell placement)
- Pre-CTS optimization
- Clock-Tree Synthesis (CTS)
- Post-CTS optimization
- Routing
- Post-routing optimization
Semiconductor Manufacturing

- Layout (GDSII stream format)
- Foundry (Semiconductor manufacturing)
  TSMC, Global Foundries, ...
- Bare dies
Semiconductor Manufacturing

• Input
  – Layout (GDSII stream format)
    • A set of geometric objects

①: Layer id 3, polygon { 50, 40, 70, 40, 70, 220, 50, 220, 50, 140, 20, 140, 20, 110, 50, 110, 50, 40 }

②: Layer id 7, rectangle { 10, 105, 40, 150 }
Semiconductor Manufacturing

Low-k CDO Dielectric

Copper Interconnects
Semiconductor Manufacturing

M3

M2

M1

p+  n+  n+  p+  p+  n+

p-epi  n-well

substrate
Semiconductor Manufacturing

p+ substrate

p-epi

p+ substrate
Gate-oxide deposition
Semiconductor Manufacturing

![Layers of semiconductor materials]

- Photoresist
- SiO$_2$
- p-epi
- p+ substrate
Semiconductor Manufacturing

Mask

SiO₂

p-epi

p+ substrate
Semiconductor Manufacturing

Expose (photolithography)

SiO₂

p-epi

p+ substrate
Semiconductor Manufacturing

After photolithography

SiO₂

p-epi

p+ substrate
Semiconductor Manufacturing

Remove mask

- SiO$_2$
- p-epi
- p+ substrate
Semiconductor Manufacturing

Etching
Semiconductor Manufacturing

Etching

p-epi

p+ substrate
Semiconductor Manufacturing

Oxide deposition
Semiconductor Manufacturing

Photoresist

p+ substrate

p-epi
Semiconductor Manufacturing

Mask

p+ substrate

p-epi
Semiconductor Manufacturing

Photolithography
After photolithography
Semiconductor Manufacturing

Etch

p+ substrate

p-epi
Semiconductor Manufacturing

Doping

- p+ substrate
- p-epi
- p+ (p-well)
Semiconductor Manufacturing

Doping

- p+ substrate
- p-epi
- n+ (n-well)
- p+ (p-well)
Semiconductor Manufacturing

n⁺ (n-well)  p⁺ (p-well)  p-epi  p⁺ substrate

Poly
Semiconductor Manufacturing

Etch
Semiconductor Manufacturing

Doping

- p+ substrate
- p-epi
- p+ (p-well)
- n+ (n-well)
- p+ (p-well)
Oxide deposition
Semiconductor Manufacturing

Contact
Semiconductor Manufacturing
Semiconductor Manufacturing

Via12
Semiconductor Manufacturing

Chemical-mechanical-polishing (CMP)
Semiconductor Manufacturing