Lecture 23

Design for Testability (DFT): Full-Scan

(Lecture 19alt in the Alternative Sequence)

- Definition
- Ad-hoc methods
- **Scan design**
  - Design rules
  - Scan register
  - Scan flip-flops
  - Scan test sequences
  - Overheads
  - Scan design system

- Summary
Definition

- **Design for testability** (DFT) refers to those design techniques that make test generation and test application cost-effective.

- **DFT methods for digital circuits:**
  - Ad-hoc methods
  - Structured methods:
    - Scan
    - Partial Scan
    - Built-in self-test (BIST)
    - Boundary scan

- **DFT method for mixed-signal circuits:**
  - Analog test bus
Ad-Hoc DFT Methods

- Good design practices learnt through experience are used as guidelines:
  - Avoid asynchronous (unclocked) feedback.
  - Make flip-flops initializable.
  - Avoid redundant gates. Avoid large fanin gates.
  - Provide test control for difficult-to-control signals.
  - Avoid gated clocks.
  - Consider ATE requirements (tristates, etc.)

- Design reviews conducted by experts or design auditing tools.

- Disadvantages of ad-hoc DFT methods:
  - Experts and tools not always available.
  - Test generation is often manual with no guarantee of high fault coverage.
  - Design iterations may be necessary.
Scan Design

- Circuit is designed using pre-specified design rules.
- Test structure (hardware) is added to the verified design:
  - Add a *test control* (TC) primary input.
  - Replace flip-flops by *scan flip-flops* (SFF) and connect to form one or more shift registers in the test mode.
  - Make input/output of each scan shift register controllable/observable from PI/PO.
- Use combinational ATPG to obtain tests for all testable faults in the combinational logic.
- Add shift register tests and convert ATPG tests into scan sequences for use in manufacturing test.
Scan Design Rules

- Use only clocked D-type of flip-flops for all state variables.
- At least one PI pin must be available for test; more pins, if available, can be used.
- All clocks must be controlled from PIs.
- Clocks must not feed data inputs of flip-flops.
Correcting a Rule Violation

- All clocks must be controlled from PIs.
Scan Flip-Flop (SFF)

- D flip-flop
  - Master latch
  - Slave latch

Logic overhead

MUX

CK

Master open Slave open

TC

Normal mode, D selected
Scan mode, SD selected
Level-Sensitive Scan-Design
Flip-Flop (LSSD-SFF)

Master latch

Slave latch

D flip-flop

MCK

TCK

SCK

SD

Logic overhead

Normal mode

Scan mode
Adding Scan Structure

Combination logic

SFF

SFF

SFF

SCANOUT

Not shown: CK or MCK/SCK feed all SFFs.
An Example

Combinational Circuit

D 1 Clk

D 2 Clk

y2

G1

F

G2

y1

G3

Z

F

y1

Y1

Y2
Inserting the Muxes

Combinational Circuit

\[ y_2 \]
\[ G_1 \]
\[ F \]
\[ D \]
\[ Q \]
\[ 0 \]
\[ 1 \]
\[ Clk \]
\[ 0 \]
\[ 1 \]
\[ Clk \]
\[ Y_2 \]
\[ Scan-out \]

\[ G_2 \]
\[ y_1 \]
\[ F \]
\[ D \]
\[ Q \]
\[ 0 \]
\[ 1 \]
\[ Clk \]
\[ 0 \]
\[ 1 \]
\[ Clk \]
\[ Z \]
\[ Scan-out \]
Comb. Test Vectors

[Diagram showing a combinational logic circuit with inputs PI, SCANIN, and TC, and outputs PO, SCANOUT, and Next state.]
### Comb. Test Vectors

**Sequence length** = \((n_{\text{comb}} + 1) n_{\text{sff}} + n_{\text{comb}}\) clock periods

- \(n_{\text{comb}}\) = number of combinational vectors
- \(n_{\text{sff}}\) = number of scan flip-flops

#### Example

<table>
<thead>
<tr>
<th>PI</th>
<th>I1</th>
<th>I2</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCANIN</td>
<td>S1</td>
<td>S2</td>
</tr>
<tr>
<td>TC</td>
<td>0 0 0 0 0 0 0</td>
<td>1 0 0 0 0 0 0</td>
</tr>
<tr>
<td>PO</td>
<td>O1</td>
<td>O2</td>
</tr>
<tr>
<td>SCANOUT</td>
<td>N1</td>
<td>N2</td>
</tr>
</tbody>
</table>

*Don’t care or random bits*
Testing Scan Register

- Scan register must be tested prior to application of scan test sequences.
- A shift sequence 00110011... of length $n_{sff}+4$ in scan mode (TC=0) produces 00, 01, 11 and 10 transitions in all flip-flops and observes the result at SCANOUT output.
- Total scan test length: \((n_{comb} + 2)n_{sff} + n_{comb} + 4\) clock periods.
- Example: 2,000 scan flip-flops, 500 comb. vectors, total scan test length ~ 10^6 clocks.
- Multiple scan registers reduce test length.
Multiple Scan Registers

- Scan flip-flops can be distributed among any number of shift registers, each having a separate scanin and scanout pin.
- Test sequence length is determined by the longest scan shift register.
- Just one test control (TC) pin is essential.
Scan Overheads

- **IO pins:** One pin necessary.

- **Area overhead:**
  - \( \text{Gate overhead} = \left[ \frac{4 \ n_{\text{sff}}}{n_g + 10 \ n_{\text{sff}}} \right] \times 100\% \), where \( n_g = \text{comb. gates} \); \( n_{\text{ff}} = \text{flip-flops} \);
  - Example – \( n_g = 100k \) gates, \( n_{\text{ff}} = 2k \) flip-flops, overhead = 6.7%.
  - More accurate estimate must consider scan wiring and layout area.

- **Performance overhead:**
  - Multiplexer delay added in combinational path; approx. two gate-delays.
  - Flip-flop output loading due to one additional fanout; approx. 5-6%.
Hierarchical Scan

- Scan flip-flops are chained within subnetworks before chaining subnetworks.
- Advantages:
  - Automatic scan insertion in netlist
  - Circuit hierarchy preserved – helps in debugging and design changes
- Disadvantage: Non-optimum chip layout.
Optimum Scan Layout

- IO pad
- Flip-flop cell
- Routing channels
- SFF cell
- TC

Active areas: XY and X’Y’
Scan Area Overhead

Linear dimensions of active area:

\[ X = \frac{(C + S)}{r} \]
\[ X' = \frac{(C + S + \alpha S)}{r} \]
\[ Y' = Y + ry = Y + Y(1 - \beta) / T \]

Area overhead

\[ \frac{X'Y' - XY}{XY} \times 100\% \]
\[ = \left( 1 - \beta \right) \]
\[ = \left( \alpha s + \frac{1}{T} \right) \times 100\% \]

\( y = \) track dimension, wire width + separation
\( C = \) total comb. cell width
\( S = \) total non-scan FF cell width
\( s = \) fractional FF cell area
\( s = \frac{S}{(C+S)} \)
\( \alpha = \) SFF cell width fractional increase
\( r = \) number of cell rows or routing channels
\( \beta = \) routing fraction in active area
\( T = \) cell height in track dimension \( y \)
Example: Scan Layout

- 2,000-gate CMOS chip
- Fractional area under flip-flop cells, $s = 0.478$
- Scan flip-flop (SFF) cell width increase, $\alpha = 0.25$
- Routing area fraction, $\beta = 0.471$
- Cell height in routing tracks, $T = 10$
- Calculated overhead = 17.24%
- Actual measured data:

<table>
<thead>
<tr>
<th>Scan implementation</th>
<th>Area overhead</th>
<th>Normalized clock rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td>0.0</td>
<td>1.00</td>
</tr>
<tr>
<td>Hierarchical</td>
<td>16.93%</td>
<td>0.87</td>
</tr>
<tr>
<td>Optimum layout</td>
<td>11.90%</td>
<td>0.91</td>
</tr>
</tbody>
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### ATPG Example: S5378

<table>
<thead>
<tr>
<th></th>
<th>Original</th>
<th>Full-scan</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of combinational gates</td>
<td>2,781</td>
<td>2,781</td>
</tr>
<tr>
<td>Number of non-scan flip-flops (10 gates each)</td>
<td>179</td>
<td>0</td>
</tr>
<tr>
<td>Number of scan flip-flops (14 gates each)</td>
<td>0</td>
<td>179</td>
</tr>
<tr>
<td>Gate overhead</td>
<td>0.0%</td>
<td>15.66%</td>
</tr>
<tr>
<td>Number of faults</td>
<td>4,603</td>
<td>4,603</td>
</tr>
<tr>
<td>PI/PO for ATPG</td>
<td>35/49</td>
<td>214/228</td>
</tr>
<tr>
<td>Fault coverage</td>
<td>70.0%</td>
<td>99.1%</td>
</tr>
<tr>
<td>Fault efficiency</td>
<td>70.9%</td>
<td>100.0%</td>
</tr>
<tr>
<td>CPU time on SUN Ultra II, 200MHz processor</td>
<td>5,533 s</td>
<td>5 s</td>
</tr>
<tr>
<td>Number of ATPG vectors</td>
<td>414</td>
<td>585</td>
</tr>
<tr>
<td>Scan sequence length</td>
<td>414</td>
<td>105,662</td>
</tr>
</tbody>
</table>
Automated Scan Design

- Behavior, RTL, and logic design and verification
- Gate-level netlist
- Combinational ATPG
  - Combinational vectors
  - Scan sequence and test program generation
  - Scan chain order
  - Test program
- Scan design rule audits
- Scan hardware insertion
  - Scan netlist
  - Chip layout: Scan-chain optimization, timing verification
- Design and test data for manufacturing
  - Mask data

Rule violations

Timing and Power

- Small delays in scan path and clock skew can cause race condition.
- Large delays in scan path require slower scan clock.
- Dynamic multiplexers: Skew between TC and TC signals can cause momentary shorting of D and SD inputs.
- Random signal activity in combinational circuit during scan can cause excessive power dissipation.
Scan is the most popular DFT technique:
- Rule-based design
- Automated DFT hardware insertion
- Combinational ATPG

Advantages:
- Design automation
- High fault coverage; helpful in diagnosis
- Hierarchical – scan-testable modules are easily combined into large scan-testable systems
- Moderate area (~10%) and speed (~5%) overheads

Disadvantages:
- Large test data volume and long test time
- Basically a slow speed (DC) test