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This tutorial is an introduction to Cadence tool for circuit layout and simulations. It deals with the layout of the circuits and their simulations using Cadence packages.

- Virtuoso for layouts
- Analog Artist Environment for design simulations.

Virtuoso is the layout editor tool of Cadence. The simulations of the designs can be done using the Analog Artist Environment.

**Logging onto the SUN systems**

At the SUN systems log in screen enter your EECS log in ID, change the environment to Common Desktop Environment (CDE) in the options menu followed by pressing OK and then enter your password followed by ENTER.

**Creating a working directory**

Once logged in successfully, open a terminal window. To do this you can do one of the following

1. Right click on the desktop and go to the Tools option, then choose Terminal.
2. Click on the button above Performance management meter on the front panel. Choose This host

Now at the prompt “gt0%”, type `mkdir Cadwork` to create a working directory named Cadwork. All the work done will be stored in this directory.

**Starting Cadence**

To start cadence, type `rca` at the command prompt. This starts Cadence in the background and you should get a window with the icfb Command Interpreter Window (CIW) as below.
The Library manager window, which looks like this, also opens.

You will also get a "What's New" window which you can read and then close or minimize.

To view the help manuals, click the Help button on the icfb window.

Creating a library

The fist task is to create a design library. To create a library, go to File→New→Library.
The following window opens. Enter the name of your library say tutorial in the text box.

If you want to store the library at a different path, enter the name in the path text box. Eg. ~/Cadwork
Next click on the radio button **Attach to an existing tech library.** This displays a drop down menu box. From the menu box choose the technology you want to use. In this tutorial we shall use TSMC 0.2u CMOS018 (6M, sblock, HV FET) technology, which is the CMOS 180nm (0.18μm) technology.

Then click the OK button. This will create a library with name tutorial, attached to TSMC 180nm technology.

Look at the Library manager window. This new library created should be an entry in it under the column Library.

*Creating a cell-view for Layout editor*

Once you have created a design library, you can start to put your design into it. In this tutorial we shall create an inverter.

Now to create a cell-view go to

File→New→Cell-view
From the drop down menu box of Library name, choose the library you want the current cell-view to be in. In the present case, it is the **tutorial** library.

Enter the name of your cell-view say **inverter** in the text box. Then choose the **Virtuoso** from the drop down menu called **Tool**. Virtuoso is the layout editor.

Clicking the OK button should open the layout editor and the LSW, which look as follows:

The LSW window contains a list of all the layers available in the technology being used (here TSMC 180nm). The layers must first be selected from this window to draw them in the layout editor.

Get acquainted with the Virtuoso Layout editor window. On the left side are various shortcuts to commonly used commands such as: save, fit, edit, zoom in and out, stretch, copy, move, delete, undo, instances, path, rectangle, ruler etc. These commands and many more can also be accessed from the menu.
**Design Inverter**
Now let us create an inverter in the editor. To create an inverter we need a PMOS transistor, an NMOS transistor. A transistor is formed by the overlap the active (p-active for PMOS and n-active for NMOS) and poly layer (polysilicon) layers. In this tutorial we shall use the MOSIS SCMOS (Scalable CMOS) scalable design rules. These design rules are $\lambda$-based designed rule set, all design rules are expressed as function of $\lambda$. Following table shows the values of $\lambda$ for various technologies.

<table>
<thead>
<tr>
<th>Technology</th>
<th>Technology name in NSCU Tool kit</th>
<th>$\lambda$ ($\mu$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMI 1.5$\mu$m</td>
<td>AMI 1.6$\mu$m ABN (2P, NPN)</td>
<td>0.8</td>
</tr>
<tr>
<td>AMI 0.5$\mu$m</td>
<td>AMI 0.6$\mu$m C5N (3M, 2P, high-res)</td>
<td>0.3</td>
</tr>
<tr>
<td>HP 0.5$\mu$m</td>
<td>HP 0.6$\mu$m AMOS14TB (3M, sblock, thixo cap)</td>
<td>0.3</td>
</tr>
<tr>
<td>TSMC 0.35$\mu$m</td>
<td>TSMC 0.4$\mu$m CMOS035 (4M,sblock,HV FET)</td>
<td>0.2</td>
</tr>
<tr>
<td>TSMC 0.25$\mu$m</td>
<td>TSMC 0.3$\mu$m CMOS025 (5M,HV FET)</td>
<td>0.15</td>
</tr>
<tr>
<td>TSMC 0.18$\mu$m</td>
<td>TSMC 0.2$\mu$m CMOS018 (6M,sblock,HV FET)</td>
<td>0.1</td>
</tr>
</tbody>
</table>

The $\lambda$ value for this tutorial is 0.1

The design rules set can be found at MOSIS’s website

In this tutorial we shall layout an inverter with PMOS and NMOS transistors of minimum size. According to the design rules the minimum length of transistor equals $2\lambda$ (the minimum width of polysilicon), while minimum width equals $3\lambda$ (the minimum width of active/diffusion).

**Layout of Inverter**

The instances of the PMOS and NMOS transistors are already available in the technology library. For an NMOS transistor, go to

Create→Instance

The following window should open
Click on **Browse** and the following **Library Browser** window should open.

Under the **Library** column choose **NSCU_TechLib_tsmc02** (this is the technology we are using) and under the **Cell** column choose the **nmos** cell and click **Close** button.

Place the instance of the NMOS transistor in the Layout Editing window as follows.

To reveal the nmos transistor with all its layers click **Shift-f** and the NMOS transistor is shown.
In the similar way obtain an instance of the PMOS transistor and place it above the NMOS transistor such that the distance between n-active layer (green) and n-well layer is 0.6 (6λ). You can use the ruler to measure the lengths in the Layout Editor window.
Since both the transistors in an inverter have the same input, we shall connect the gates with polysilicon layer. Choose the **poly** layer and draw a rectangle as shown in the following figure. In the inverter, the output terminal is the contact of the drains of the two transistors. Draw a rectangle of metall layer and place it such that it touches the metal layers of the contacts in the two transistors.
Now for the power and ground rails, draw two *metal1* rectangles and place those at 0.3 unit distance from two active regions, as shown in figure. Connect these two metal layers to the source of the transistors with metal1 layer to complete the contact between the transistor and power rails.

The bulks of the two transistors must be connected to proper voltages. Here the n-well of PMOS must be tied to Vdd while the bulk of NMOS must be tied to ground. Goto Create→Contact. From the drop down box choose M1_N contact and place it on the power rail as shown in figure. Goto Create→Contact. From the drop down box choose M1_P contact and place it on the ground rail as shown in figure. To reveal the contacts press Shift-f and to hide them press Ctrl-f.
The M1_N contact must be inside the n-well, so draw a rectangle with n-well layer so that it encloses the contact by at least 0.1 units on all sides.

It is a good practice to periodically keep checking for design rule errors. Goto Verify→DRC. The following window appears.

Finish by clicking OK. If any design rules have been violated, they would be marked on the layout. Usually a simple rule violation could result in multiple errors.

Now we shall create pins to mark the input terminal, output terminal, VDD and GND. Goto Create→Pin, the following window appears.
In the Terminal Names field enter the following labels: In, Out, VDD, GND. For Mode select sym pin (if it is not already selected). Select Display Pin Name, for I/O Type select input and chose poly for Pin Type. Now move the cursor to the Virtuoso window, you will find that it now carries a rectangle box with “In” letters. Place it at the mid point of the polysilicon layer. Clicking once places the poly layer and a second click of the left mouse button ensures that the label is attached to the layer. Go to the Create⇒Pin form and change I/O Type to output and the Pin Type to metall1. Move the cursor back to the Virtuoso editor and place this layer at the center of the metall1 layer that connects the transistor Drains. Click once to place the layer and one more time to attach the label. Go to the Create⇒Pin form and change I/O Type to input. Back on the Virtuoso editing window place this pin at the center of the metall1 layer (power rail) above the p-type transistor. Click once to place the layer and second time to attach the Vdd label. Repeat the above procedure to attach the gnd label on the metall1 layer below the n-type transistor. The Pin type must be same as the layer on which they are place.

Click on the Save button or go to Design⇒Save to save the layout.
Run the DRC again and if any design rule violations occur, correct them. Repeat this until there are no errors. Ones the DRC is passed, goto Verify⇒Extract.
Click on the Set Switches button and select Extract_parasitic_caps, and keep_labels_in_extracted_view
and click OK. The rest of the information in this window should be correct by default, finish by clicking
OK. This should create an extracted view of the inverter layout. Simulation can be performed on
this view. To open the extracted view, in the library manager window, select the library “Tutorial”
under library column, “inverter” in the cell column, and double click on “extracted view” in the view
column. The following window should open.

Simulation

For the simulations of the designs we use the Analog Artist Environment tool. In the Virtuoso
Layout Editing window of the extracted view, start by going to Tools→Analog Environment.
This will open the Affirma Artist Circuit Design Environment simulation window, which is as
shown below.
The design should be set to the right Library, Cell and View.

Now go to Setup→Simulator/Directory/Host.

From the window that opens up select the simulation type as spectreS from the drop down menu. Finish by clicking OK. Then go to Setup→Stimulus→Edit Analog. From window that opens up choose the radio button graphical and click OK.

The window shown below opens. This is the window in which the stimulus to the inverter is defined. Observe that the inputs defined in our layout are the entries in this window.

Click on OFF IN/gnd! Voltage dc, in the text box. Change the Function to a pulse. And enter the pulse parameters as shown and click the change button. Observe the input IN change from off to on.
Now select and enable the Vdd input, give it a dc value of 5V and click the change button. Observe Vdd change from off to on. Finish by clicking OK. Similarly give gnd a dc value of 0.

Next we have to give the type of analysis to be performed. Let us perform a transient analysis for 20ns. So go to Analysis→Choose or click the second button on the right of the window. Click the transient analysis radio button and enter the stop time as 20n. Finish by clicking OK.
Now we have to choose the outputs to be plotted in the waveform viewer.
Go to Outputs→To be plotted→Select on schematic.
Then the editor window automatically comes into focus. Click on the polysilicon layer for input and metal layer for output. Notice that these metal layers are highlighted. Go back to the Analog Artist Environment window and now there are two entries in the output section of the window. These are the signals that will be displayed. To start the simulations click on the button showing the traffic light (with green). After simulations are done the waveform window opens and displays the signals IN and OUT as shown.

Click on this button Switch Axis mode in the waveform viewer to display the waveforms separately. You can use the crosshair to make measurements on the waveforms. They can be obtained by clicking the buttons Crosshair marker A, Crosshair marker B or using the hot keys a and b.
The netlist generated by the simulator can be viewed by going to Simulation→Netlist→Display Final Netlist.

It is a good idea to save the state of simulation, if you want to redo any of the simulations without having to re-enter everything from scratch. To save the current state of the simulation, in the Analog Artist Environment window go to Session→Save state. In the window that opens, enter the name for the state of simulation to be saved.

To redo a saved simulation, follow this procedure. When the Analog Artist Environment window opens, go to Setup→Simulation.

From the window that opens select the simulation type as SpectreS from the drop down menu. Finish by clicking OK. Then go to Session→Load state. A window as follows opens.

From this select the state you want to load and finish by clicking OK. The previously saved state of simulation is loaded and you can make any changes if needed and continue with simulation.